Mixed Signal Design Guide

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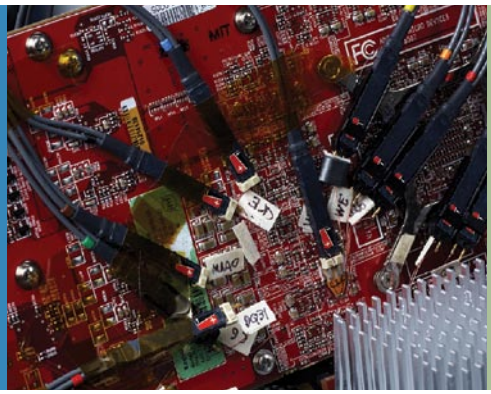

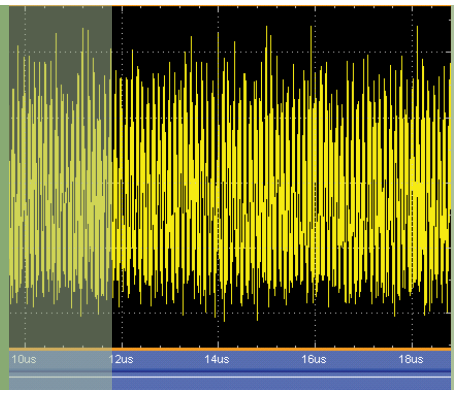

Debug and Validation of High Performance Mixed Signal Designs

Application Note

Introduction

Modern embedded and computing systems have become progressively more powerful by incorporating high-speed buses, industry standard subsystems, and more integrated functionality in chips. They have also become more complex, more sensitive to signal quality, and more time consuming to troubleshoot.

While standards exist for many technologies commonly used within high performance digital systems, a major test requirement is to ensure that all elements are synchronized and perform as a seamless, integrated whole. End devices may contain multiple subsystems, some of which need to communicate with one another and with the outside world. This is an extension of integration testing where the timing of integrated functions and communication between subsystems must be verified. This testing requires tools that enable evaluation of not only a single element but also an entire system.

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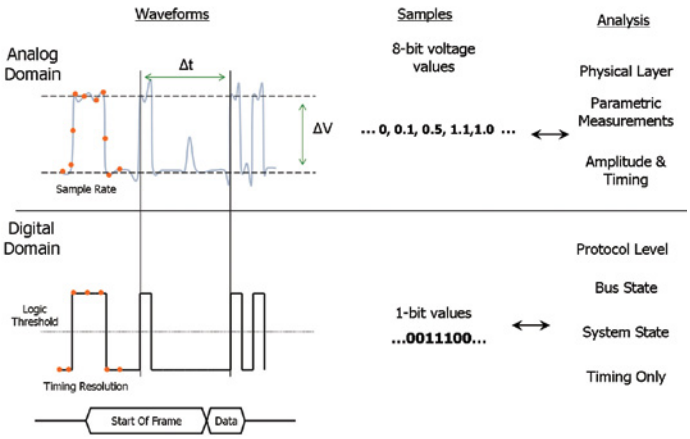

Figure 1. Analog and digital measurement differences.

Figure 2. MSO70000 can provide time correlated views of analog and digital signals.

System testing overview

In step with increasing functionality and performance, engineers often have to work with both analog and digital signals in their designs. This complicates the job of testing, requiring specialized tools to see what is happening at various test points on the device under test. Analog testing, for example, requires precise voltage values for performing physical layer analysis such as amplitude, timing or eye diagram measurements. The oscilloscope has been the primary tool for this job. Digital system test uses only logic state values and may use timing information only. By time correlating many digital signals bus or protocol level analysis can be performed. Digital system test and debug may require triggering on specific bus cycles such as a memory read or write. Logic analyzers with wide bus capabilities are typically used for digital system test.

In many cases, when hardware and software engineers are working together to troubleshoot the root cause of a specific problem, they require a view of information on a bus - both its electrical representation and also at a higher level of abstraction like the decoded view of a serial bus protocol. Many designs have a large number of hardware components for executing specific tasks that may be located on different parts of the circuit board. To verify interaction between components, engineers need to have a system-level view of the DUT. The challenge is to make sure that the component operations are synchronized, which means that the test equipment needs to be able to provide accurate information on timing performance in addition to viewing and analyzing data at higher levels of abstraction and analysis.

A mixed-signal oscilloscope (MSO) provides analog signal characterization with digital bus event and timing analysis for the ideal system debugging tool. Mixed analog and digital design and validation benefits from three key MSO capabilities: timing correlation, state visibility, and data qualification.

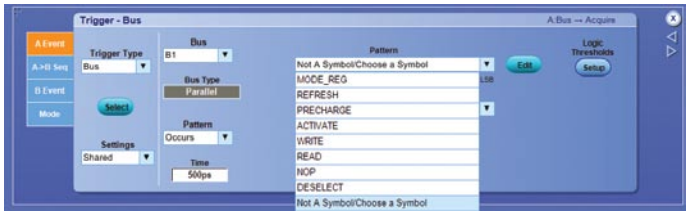

Figure 3. Triggering with user-definable Bus definitions.

Figure 4. Bus qualified trigger of memory read cycle.

Analog and Digital Correlation

Time-correlated analog and digital signal information can lead to more efficient verification and debugging. In mixed-signal control systems, software-based control loop behavior can be correlated with analog stimulus and response signals. In system debugging, incorrect digital states (e.g. invalid character) can be more easily traced to low-level signal effects (e.g. data dependent jitter) in the physical layer.

Understanding the context in which an event occurred can be valuable while debugging digital systems. For example, what memory location was being accessed? Where did this packet of information originate? What was the state of the ASIC when that bus fault occurred? Low-level or physical layer details are often needed to identify root cause but often the most efficient way to trace issues is to understand in what state was the larger system. Being able to capture several views of signaling as it flows through a system can more quickly lead to critical insight.

Often it is necessary to analyze specific cycle types, such as signal integrity during read cycles or write timing jitter for a specific bank of memory. Sophisticated signaling schemes such as in DDR can complicate debugging. When cycle information is distributed across several digital signals it takes sophisticated triggering to respond to it in real time. Thus, effective debugging may include detecting signal faults only during specific bus cycles. Digital pattern qualification can be applied to logic-fault trigger types to detect signal faults in real time, such as a glitch during a Read.

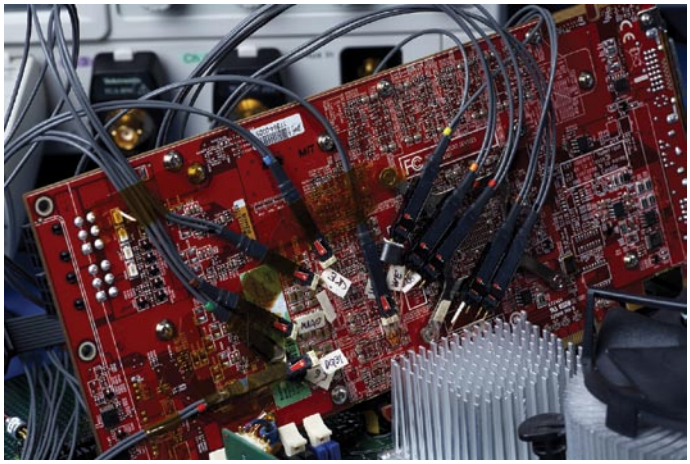

Figure 5. P6780 differential logic probes connected to GDDR5 video graphics card.

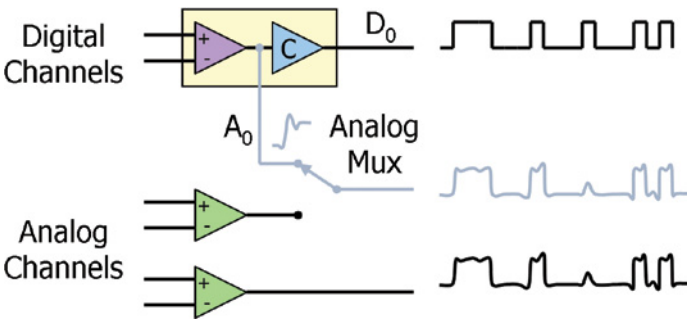

Figure 6a. Block diagram of Analog Mux.

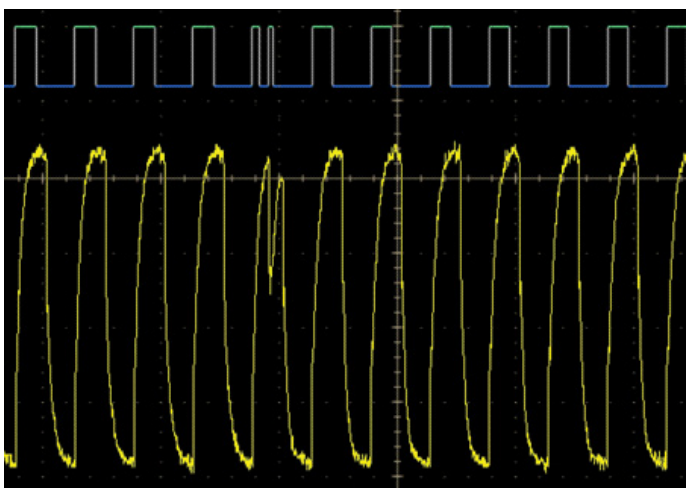

Figure 6b. Glitch shown in digital and analog view using iCapture. Both the digital and analog signals were acquired from a single probe.

Signal Access

Attaching a probe to a device poses another challenge. The small physical size of the devices, the large number of points on the board that need to be probed, and the fact that any probe adds capacitive loading altering the operational characteristics of the device are all factors that add to probing challenges. Probing solutions need to be designed to minimize the capacitive loading, make it easier for the engineer to connect to the device, and also be able to quickly ascertain which probe (or probe lead) is correlated to which trace on the screen of a test instrument.

The MSO70000 series Mixed Signal Oscilloscopes provide high performance, 16 channel logic probes like the P6780 Differential Logic Probe. The P6780 can connect to small vias and components using accessories designed for solder-in connections.

Analog Mux

The MSO70000 series includes the iCapture analog mux feature that allows engineers to view a signal connected to any of the 16 logic probe connections in simultaneous analog and digital views. There are two key benefits of the iCapture capability. First double probing is not required to view signals in both digital and analog domain. This helps ensure optimum signal fidelity of the device under test by reducing the capacitive loading introduced by the test equipment. The second benefit is improved timing and precision that is available across any of the 16 digital channels. The user can turn on the analog signal through the oscilloscope's user interface or develop software routines to turn on or off the analog mux in an automated fashion.

Mixed Analog and Digital Devices

Mixed signal design problems are difficult to debug and often require advanced measurement techniques across multiple domains. The MSO70000 provides both the analog and digital signal analysis capability to examine the interaction of the hardware and software in a target system. The following are three examples of using the MSO7000 to debug mixed analog and digital systems including high speed serial technologies, FPGA designs, and RF subsystems.

High Speed Serial Designs

High speed serial bus architectures, including PCI-Express, HDMI and SATA, provide significant data throughput with additional benefits such as differential signaling, lower pin count and less space for board layout. What all these latest standards have in common are faster edge rates and narrower data pulses, which combine to create unique, exacting demands on designers. As multi-gigabit data rates become common in digital systems, signal integrity - the quality of the signal necessary for proper operation of an integrated circuit - is becoming a paramount concern for designers. One bad bit in the data stream can have a dramatic impact on the outcome of an instruction or transaction.

High performance video systems can incorporate a wide variety of technologies such as RF receivers, video processors, memory and high speed serial interfaces. Figure 7 shows a typical block diagram of a high end set top box. This system has implemented an HDMI interface which operates at 3.4 Gb/s across each of the three data lanes. Figure 8 shows the architecture of the HDMI link including high speed clock and data lines along with the Display Data Channel (DDC) which uses I^2C signaling in standard mode (10 MHz). The DDC line is used for information exchange between the Source (Transmitter) and Sink (Receiver) devices.

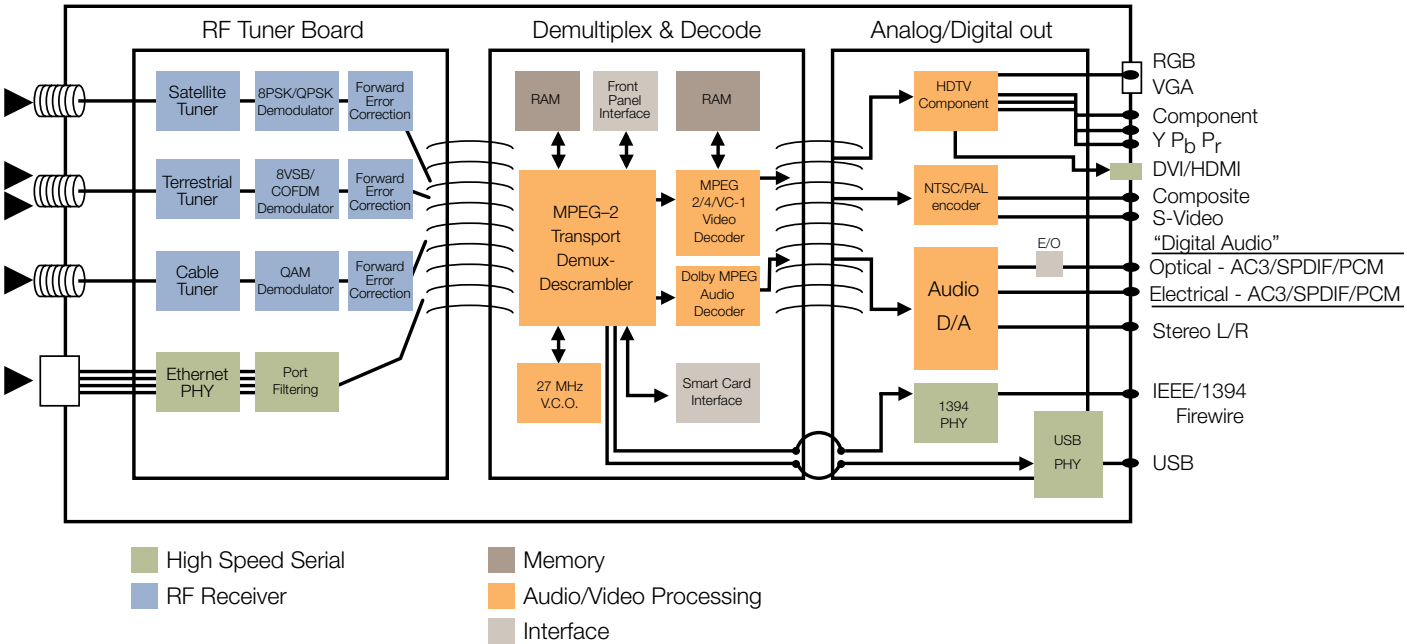

Figure 7. A block diagram of a typical HD Set Top Box.

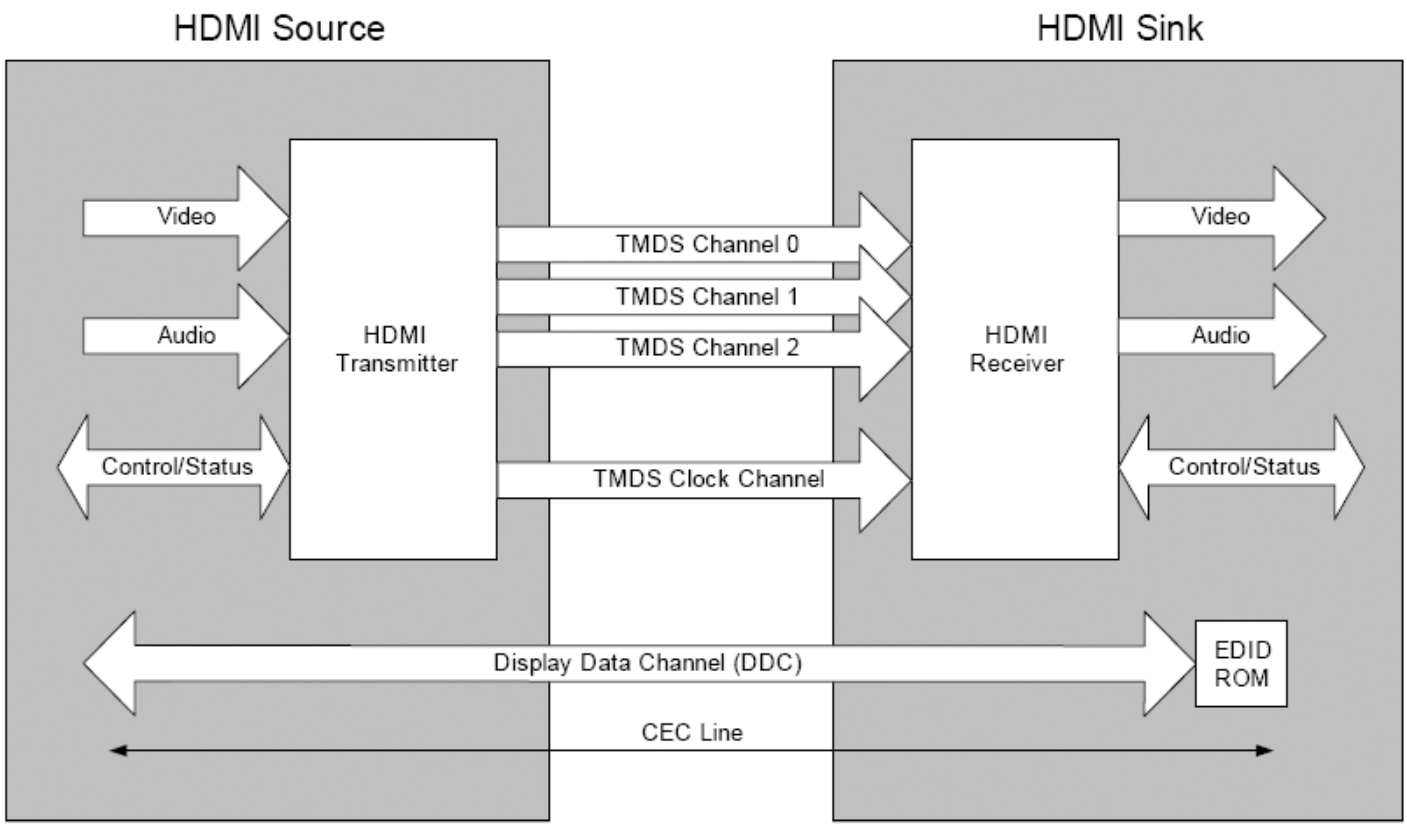

Figure 8. HDMI system architecture.

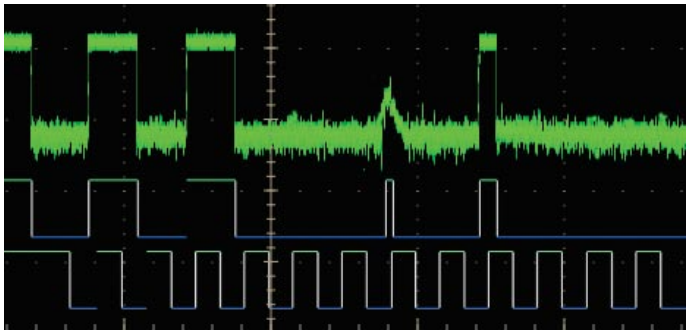

Figure 9. Glitch on I²C SDATA line.

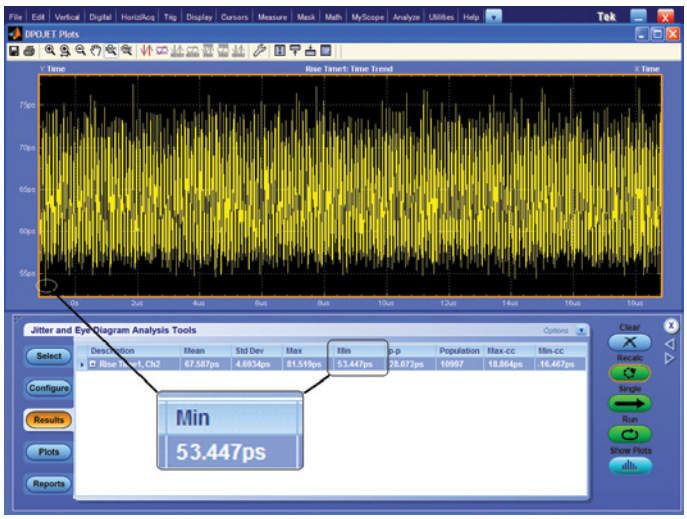

Figure 10. Trend plot of rise times within a 19 us window near the I²C glitch. The fastest edge rate measured is about 53 ps.

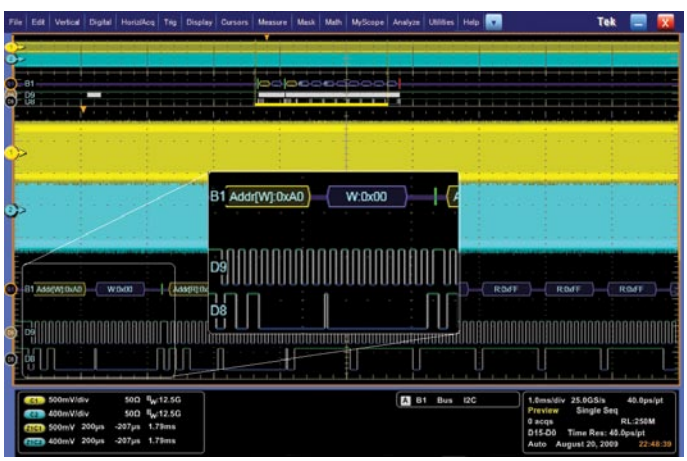

Figure 11. MSO70000 decodes address 0xA0 after crosstalk issue is resolved.

This design required debug as the output to the monitor would turn off intermittently. First the physical layer was checked for functional operation and each lane passed eye diagram and jitter measurements. After the high speed clock and data lines were measured, the I²C control lines were monitored for error codes or invalid data. In normal operation the DDC uses addresses 0xA0 and 0xA1. However after the MSO70000 captured and decoded the I²C traffic an incorrect address would sometimes be asserted during power up. Figure 9 shows the SDATA line in digital and analog format using the iCapture tool on the MSO70000. Based on the analog signal view it appeared there were crosstalk or other noise coupling effects that corrupted the I²C traffic.

In order to find the root cause of the glitch adjacent lanes were analyzed and edge rates were evaluated across each high speed lane. Figure 10 shows a 19 us time window with a trend plot of edges occurring close to the glitch. This analysis provides some insight into what caused the signal anomaly. The minimum measured rise time of 53 ps was much faster than the 90 to 100 ps edge rates typically found in HDMI systems. The design was then modified to slow the edge rates and the data and clock shielding lines were also improved. Figure 11 shows the correct I²C transactions, including addresses 0xA0 and 0xA1 and the acknowledgement bit before the Write data.

Field Programmable Gate Arrays (FPGA)

The phenomenal growth in design size and complexity continues to make the process of design verification a critical bottleneck for systems based on Field Programmable Gate Arrays (FPGAs). Limited access to internal signals, advanced FPGA packages, and printed circuit board (PCB) electrical noise are all contributing factors in making design debug and verification the most difficult process of the design cycle.

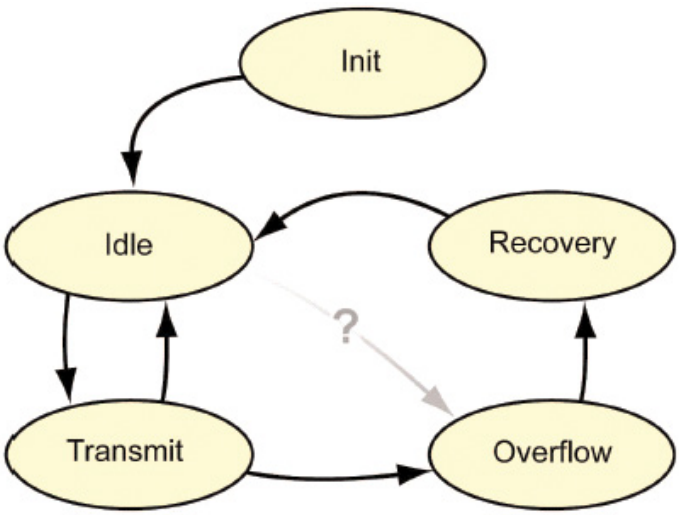

Figure 12. Debug Port state machine of the PCI Express receiver.

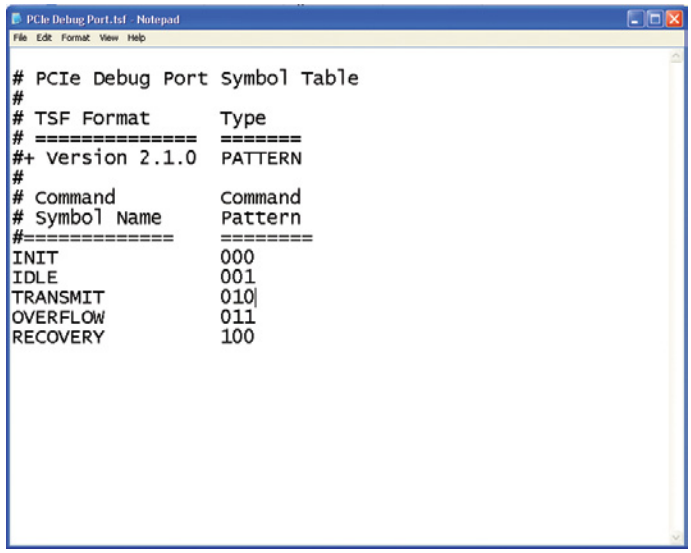

Figure 13. Tektronix symbol file for PCIe Debug Port.

When faults occur in FPGA based designs, engineers can use the MSO70000 to see analog events such as the input and output signals and power supply lines in addition to the digital lines that show them internal status of the FPGA logic. Potential problems that can be debugged include:

- Situations that were not accounted for in simulation, e.g. a power supply problem
- Cross-talk between high speed lines caused by a stronger line driver affecting an adjacent line that only occur when a set of drivers turn on together
- Incorrect SW commands sent to an state machine resulting in unexpected behavior
- State machine logic errors, unlocked phase lock loops, and FIFO overruns

Let's see how the MSO70000 was able to debug an FPGA used as a bridge between a PCI Express link and DDR memory bus. This example shows how monitoring FPGA states externally can speed debug of state machine problems in FPGAs.

PCI Express transmitter/receiver pairs often include not only a serial link, but also a built-in “debug port.” This parallel output delivers real-time data summarizing the transactions occurring within the device. With debug ports on both the transmitter and the receiver, developers can monitor the health of the transmission link and localize many types of problems to either the transmit or the receive side. Figure 12 represents a state machine that might be found within a PCI Express serial receiver. The simplified interactions shown here symbolize a routine link procedure, with the black arrows indicating legal state transitions. Figure 13 is a screen image showing an example Tektronix symbol file (.tsf) created in Notepad to enable analysis of the Debug Port on the MSO70000. Figure 14 shows an acquisition taken from a PCI Express serial link. An error on the bus has caused the MSO to trigger on bus violation. Because of the good signal quality we can visually tell the problem does not stem from an underlying analog problem. The finding in Figure 14 strongly implies a logic issue caused by a timing problem or other digital conflicts.

Because the serial data errors coincide with the Overflow state on the debug port, and because the serial data is driven by the SERDES it is reasonable to assume that the problem is timing-related and originates within the SERDES. At this point there may be several potential troubleshooting strategies, influenced by architectural considerations or other debug findings.

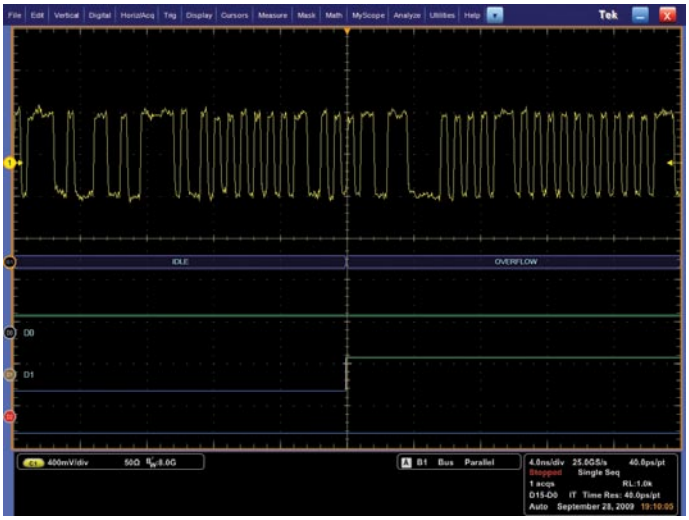

Figure 14. The bus error (OVERFLOW state) coincides with an incorrect state change in the Debug Port state machine. This implies a timing problem within the SERDES, which may stem from errors in the FPGA synthesis process.

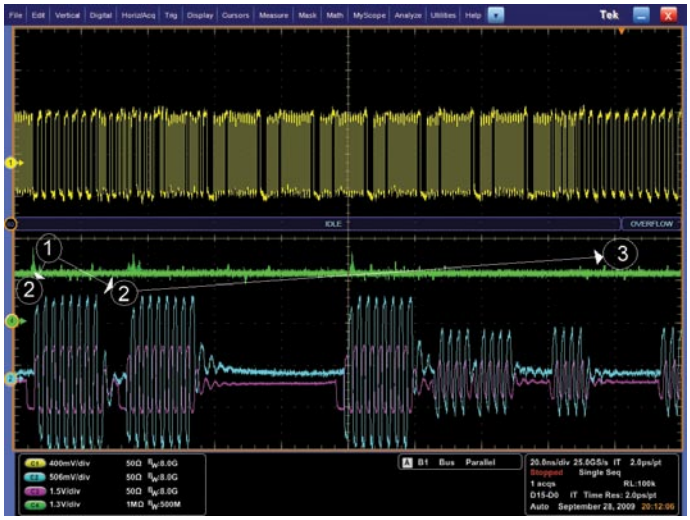

Figure 15. Ground bounce (1) causes setup and hold violations on Read data (2) which returns invalid data to PCIe bus.

In an FPGA the design is transformed into functional elements defined by the programmer. This "transformation" process is known as synthesis, since it literally synthesizes the desired functions using its internal gates. Knowing this, the astute designer will troubleshoot the error first by double-checking the FPGA synthesis results to make sure the timing of all state machine transitions is correctly implemented.

If that doesn't reveal the problem's source, a second pragmatic step is to route other signals to the debug connector to trace the device's behavior. For example, after evaluating the Current State data as shown in Figure 12 the FPGA might be reprogrammed to deliver the "Next State" data to the debug port. This could reveal issues that are not seen in the Current State, and of course there are even more states that can be investigated beyond that.

Another common approach to debugging FPGA designs is to follow the data flow backwards from the error source to determine root cause. After further investigation the MSO70000 was able to show that a power supply lin was inducing noise on the DDR memory bus. Right before the FPGA state machine put the PCIe link into an Idle state a memory Read request was issued. Switching noise caused issues with the memory bus which in turn propagated back into the PCIe bus. This was the primary cause of the FPGA state machine error.

Frequently, tracing a system problem involves much more than just following a glitch back to its source in some logic element. An error on one bus may have its origins—and its impacts—on multiple buses in the system. For this reason, complete cross-bus analysis has become an indispensable troubleshooting methodology. With the MSO70000, time-correlated digital and analog events are brought into view on a common screen, thus providing a powerful new tool in troubleshooting FPGAs and multi-bus systems. Cross-bus analysis makes it possible to see simultaneous interactions throughout the system, speeding efforts to track down not just errors, but also their root causes.

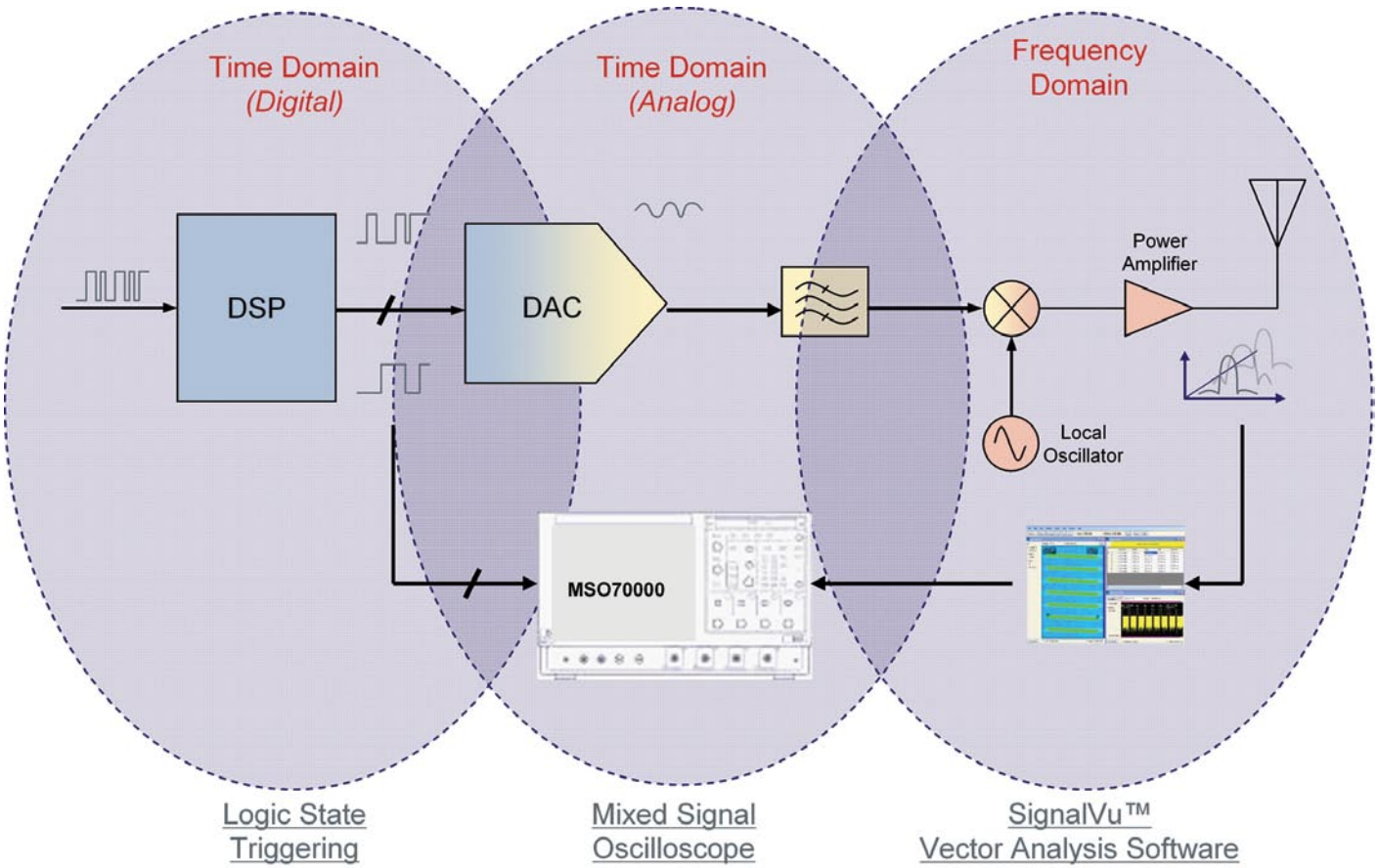

Figure 16. Block diagram of a transmitter and connectivity to a Mixed Signal Oscilloscope.

RF Test

One of the challenges in the design of software defined radios is troubleshooting and mitigation of hardware and software errors. As DSP controls more and more of the analog functionality, illegal state or filter values in the digital baseband portion of a design can manifest themselves as RF spectrum errors when they are propagated to the filtering and amplifier portions of a transmitter.

Figure 16 shows the connectivity of the MSO for complex multi-domain analysis. Not only can the digital and analog domains be analyzed, but with the inclusion of vector signal analysis software, a thorough analysis that includes the frequency domain can be performed on the same data acquisition.

For this example, the MSO logic trigger is set to catch an illegal state value to the input of the Digital-to-Analog Converter (DAC). The logic trigger for an all “1” state value (0x3F) triggers the acquisition. The correlated view of the analog signal in Figure 17 is shown delayed in time, about 34 ns. This represents the absolute delay in the DAC conversion process of this high-speed device.

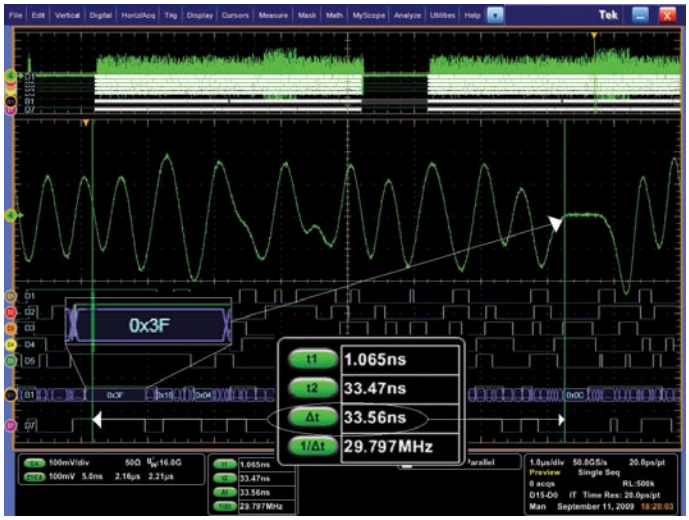

Figure 17. The integrated view of the logic states at the DAC and Analog output.

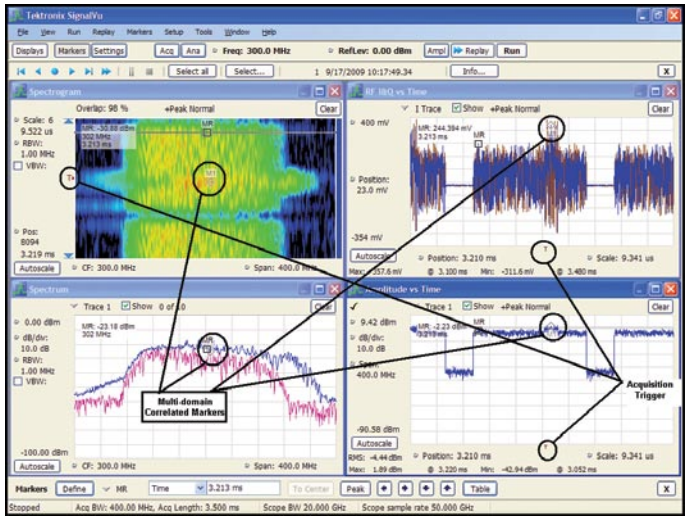

Figure 18. SignalVu enables time correlated multi-domain views for in-depth analysis.

This analysis enables the correlation of the logic state to the wide pulse appearing on the MSO's analog channel. The time domain view of the RF signal may not give us the complete view of the impact this might have on our software radio design, so further correlated analysis of the RF performance is required.

To assess the RF performance of the signal on the same acquisition, SignalVu™ software can be used directly on the same data set. Figure 18 shows RF analysis on the same data set acquired for Figure 17. The logic state trigger has been used to trigger the data set and the SignalVu analysis performs the RF analysis.

In this example, Discrete Fourier Transforms (DFTs) are performed to show the Spectrogram and Spectrum frequency domain analysis, and time sampled data is displayed as RF I&Q vs Time and Amplitude vs Time.

Time correlated markers have been turned on to demonstrate the time-correlation of the RF analysis for different views. It can clearly be seen that the illegal state values triggered at the DAC resulted in a spectral regrowth at RF. The RF regrowth can be traced back to the digital state in the block diagram, thus ruling out a hardware problem in the analog portion of the transmitter.

Summary

Digital designers need to quickly find and analyze a wide range of problems from signal integrity issues such as cross-talk or jitter to bus faults such as setup and hold violations or dropped packets. The MSO70000 Series with 80 ps timing resolution can make precise timing measurements on as many as 20 channels simultaneously. With iCapture, you can quickly view analog characteristics of a digital channel without adding another probe, saving time and minimizing load on the device under test. By triggering and decoding on a bus, invalid states are quickly detected.

High performance digital systems continue to evolve and become more complex, more sensitive to signal quality, and more time consuming to troubleshoot. An MSO can be the right tool to help efficiently analyze and debug systems and bring products to market even faster.

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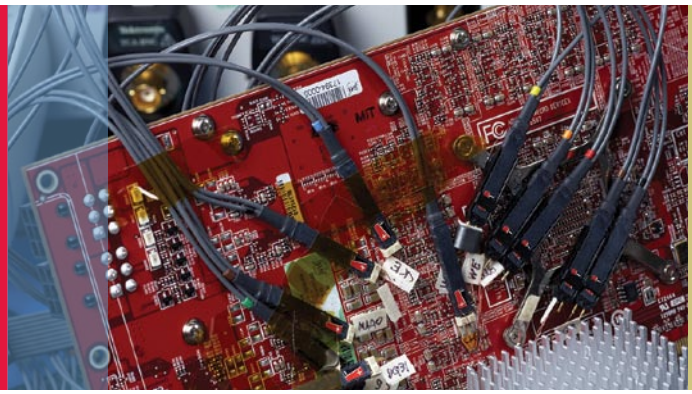

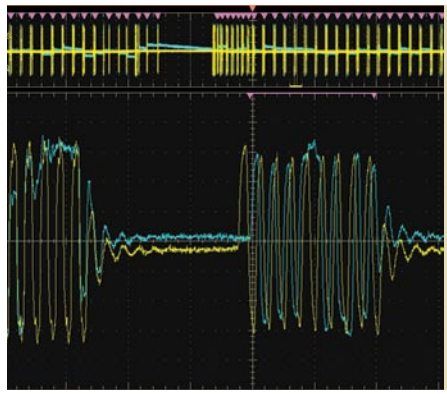

Electrical Verification of DDR Memory

Application Note

Virtually every electronic device, from smart phones to server farms, uses some form of RAM memory. Although flash NAND continues to grow because of its popularity for a wide variety of consumer electronics, SDRAM is still the dominant memory technology for most types of computers and computer-based products, offering a good combination of speed and storage capacity for relatively low cost per bit. DDR, or double-data-rate SDRAM, has become today's memory technology of choice, and the technology continues to evolve as companies strive to increase speed and capacity while reducing cost, power budget, and physical size of memory devices.

As clock rates and data transfer speeds continue to increase with each advance in performance, analog signal integrity of the memory subsystem has become an increasing area of focus for designers who must guarantee system performance margins, or ensure interoperability of memory and memory-control devices within a system. Many performance problems, even ones found at the protocol layer, can be traced back to signal integrity issues. So the importance of doing analog verification on memory devices has grown to become a critical step in validating many electronic designs.

The jitter, timing, and electrical signal-quality tests required to validate memory devices have been specified in detail by JEDEC, the Joint Electron Device Engineering Committee. Parameters such as clock jitter, setup and hold timing, signal overshoot, undershoot, transition voltages etc are included in the comprehensive set of tests described in the JEDEC specifications for each memory technology. But performing these tests in conformance with the spec presents a host of challenges that can be a complex and time-consuming task. Having the right tools and techniques can significantly reduce test time and ensure the most accurate results. In the balance of this application note, we will discuss several elements of the Tektronix solution 'toolkit' for memory test that can help overcome the inherent challenges and simplify the validation process.

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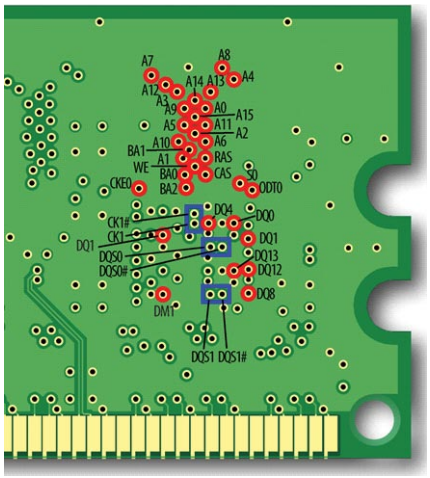


Figure 1. Test points on "back side" vias of DDR3 DIMM.

Signal Access and Probing

One of the first obstacles to overcome in memory validation is the issue of accessing and acquiring the necessary signals. The JEDEC standards specify that measurements should be made at the BGA ballouts of the memory component. Since FBGA components include an array of solder ball connections that are, for practical purposes, inaccessible, how can this be accomplished?

One solution is to design for test during PCB layout and include vias directly beneath the memory components that can be probed on the back side of the board. Although these test points are not strictly "at the component ballouts," for practical purposes the trace length through the PCB is generally short enough that signal degradation effects are minor. When this approach can be used, signal integrity is usually quite good and electrical validation can be performed with acceptable test margins.

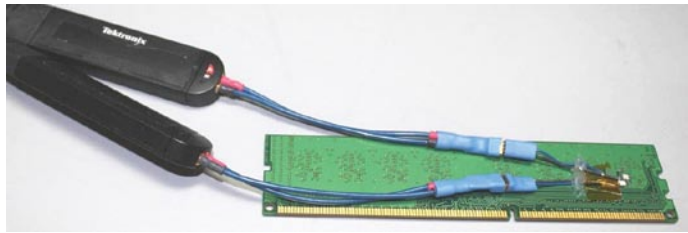


Figure 2. P7500 Micro-Coax probe tips soldered to DIMM.

Technology	JEDEC Specification (most recent update)
DDR	JESD79F (February 2008)
DDR2	JESD79-2E (April 2008)
DDR3	JESD79-3C (November 2008)
LPDDR	JESD79-4A (April 2007)
LPDDR2	JESD209-2 (March 2009)

Table 1. JEDEC Specifications for DDR Technologies.

Although it is possible to use handheld probes for this type of application, maintaining good electrical contact between multiple probe tips and test points simultaneously can be difficult. Considering that some JEDEC measurements require three or more test points, plus other signals such as Chip Select, RAS, and CAS that may be needed to qualify the memory state, the option of using solder-down probe connections quickly becomes an attractive alternative for many engineers.

Tektronix has developed a selection of probing solutions that are designed specially for this type of application. The P7500 series probes, with bandwidths from 4 GHz to 20 GHz, are the models of choice for memory applications. Figure 2 illustrates one of several available P7500 probe tips that are well-suited to memory applications. These "micro-coax" tips provide a cost-effective solution for situations where multiple tips must be soldered and left in place, while offering excellent signal fidelity and bandwidth up to 4 GHz, more than sufficient for testing memory devices up to DDR3 @ 1600 MT/s.

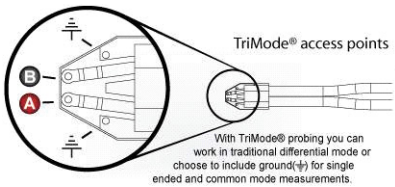


Figure 3. P7500 TriMode tip connections.

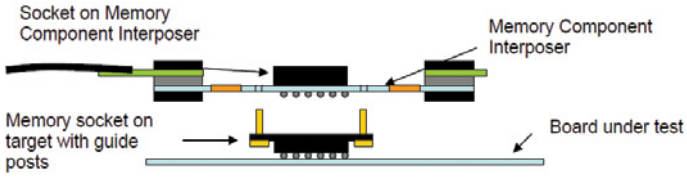
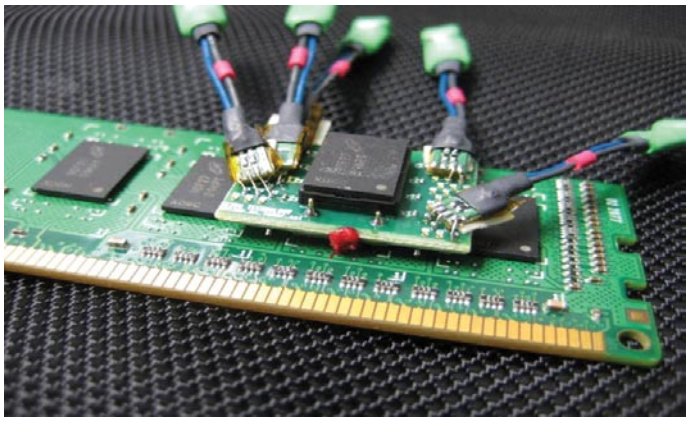


Figure 4. Component Interposer for DDR.

Another advantage of the P7500 probes for memory applications is their patented TriMode® feature. This unique feature allows the probe to measure either differentially between + and - , or single-ended between signal and ground. Using three solder connections at the probe tip, the user then has the ability to switch between differential and single-ended modes using control buttons on the probe or menu commands on the oscilloscope. One example of how this can be useful for memory applications is the technique of soldering the probe's + connection to a single-ended data or address line, and soldering the probe's – connection to another adjacent line. The user can then easily measure either of these two signals using one probe, by switching the probe between its two single-ended measurement modes.

There are, however, many situations where signal access through back-side vias may not be an option. Designs using embedded memory may not have the luxury of available board space on the back side opposite the memory components. Even many standard DIMM's now have memory components back-to-back on both sides of the board, to increase storage density. How can the test engineer get access to test points in this scenario?

Fortunately, there are now probing solutions for even this situation. Tektronix has partnered with Nexus Technologies, Inc. to develop component interposers for all standard DDR3 and DDR2 memory devices. These interposers use a socket that solders down onto the target device in place of the memory component. The interposer, which has test points for probing, then snaps into place on the socket. The memory component then attaches to the top of the interposer. Figure 4 illustrates this "stacked" arrangement.



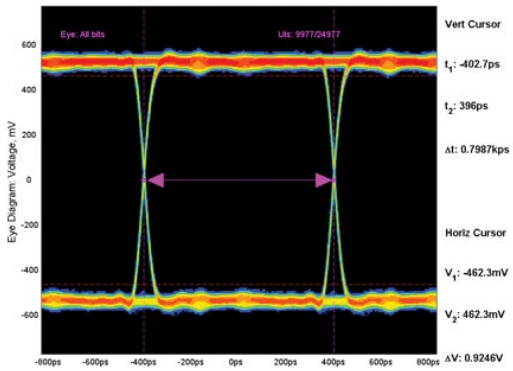


Figure 5. Component Interposer with solder tips; eye diagram of probed signal.

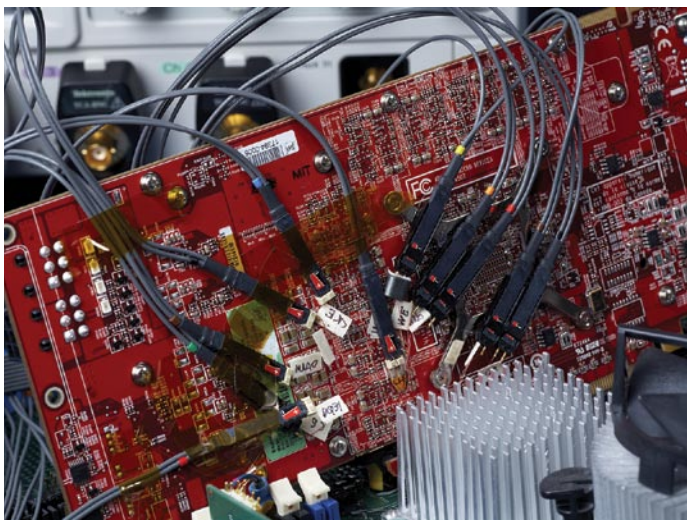


Figure 6. P6780 digital probe tips soldered onto GDDR5 PCB.

A unique feature of the Nexus interposers is the use of a patented socket that mates to and retains each of the solder balls on the component. This allows both the interposer and the memory component to be removed and replaced without un-soldering and re-soldering, giving increased versatility while also decreasing the risk of poor electrical connections inherent with multiple soldering operations.

Small isolation resistors are embedded within the interposer, as close as possible to the BGA pads of the memory component. These resistors are matched to the P7500 probe tip's electrical network, ensuring excellent signal fidelity. The eye diagram in Figure 5 was made with the interposer mounted on a DDR3-1333 DIMM similar to the one shown in the photograph, using digital filtering that removes even the small analog effects introduced by this probing setup.

Digital Probing

The Tektronix MSO70000 Series Mixed-Signal Oscilloscopes combine four analog channels with up to sixteen digital channels. In addition to connecting to 1 or 2 data and clock lines, it's often useful to connect to the DDR command bus signals and subsequent address lines. The P6780 differential probe enables high-bandwidth performance with wide bus signal access for use on the MSO70000 Series. Because of high-density layout and constrained packaging, signal access continues to be challenging for those validating DDR memory.

Probing a full spectrum of connectors, pins, device leads, traces, and vias is simplified with these high performance P6780 logic probes that include a range of solder-in accessories. With solder-in probe tips for the P6780, designers can add test points as necessary without the need to include a dedicated probe footprint. As with any measurement setup, care should be taken to minimize test equipment impact on the measurements. The P6780 solder-in tips include ferrite cores to reduce reflections on the line. Keeping wire length to the minimum required for connectivity will ensure better signal fidelity.

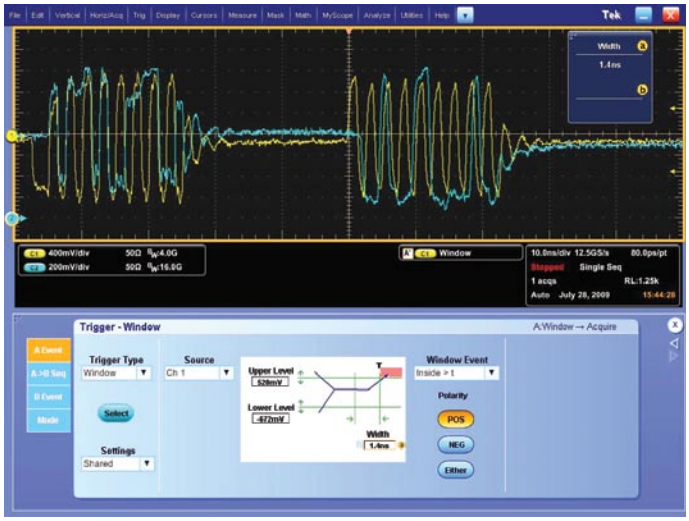


Figure 7. Using « Window » trigger to identify DQS Write Preamble.

Figure 8. Using Advanced Search & Mark to identify all write bursts.

Signal Capture

Once the signal lines have been successfully probed, the next step is to isolate the events of interest on the memory bus. If performing JEDEC conformance measurements, you may need to perform certain measurements only on qualified portions of the data stream such as read or write bursts. For debug it may be necessary to further isolate certain events by a particular rank or bank, or to isolate certain data patterns for analysis of signal-integrity issues such as data-dependent jitter, timing, or noise problems.

There are several methods that can be used to identify and isolate read- and write bursts or other bus conditions. One of the simplest methods is to use the DQS or Data Strobe signal to identify the start of a read or write burst. For example, DDR3 always asserts DQS high at the start of a write, or low at the start of a read. Hardware triggering capabilities in the oscilloscope can trigger on this preamble portion of the burst and assure that only reads or writes are captured at the beginning of the acquired waveform. Figure 7 shows both read & write bursts, with the trigger point at center-screen on a write burst.

Qualifying Reads & Writes with Advanced Search & Mark

Another tool available in the DPO/DSA70000 and MSO70000 series oscilloscopes is a software utility called Advanced Search & Mark (Option ASM). ASM can scan through an entire waveform acquisition and search for a variety of user-configurable conditions. One of these conditions available to the user is DDR Read /Write identification; ASM will find all read bursts or write bursts in an acquired waveform record and mark each burst with a visible marker on-screen. In addition to using these marks for visual analysis, the oscilloscope can apply the marks as qualifiers for DDR-specific measurements, so that measurement occurs only on the appropriate portion of the data stream. In the case of DDR, the search algorithms in ASM make use of the fact that phase relationships are different for read and write bursts; DQ and DQS are in-phase for reads, and 90 degrees out of phase for writes. In Figure 8, ASM has marked all write bursts with pink triangle symbols shown above the waveform, and a single write burst magnified in the zoom window in Figure 8.

Command	SO#	RAS#	CAS#	WE#
Mode Register	0	0	0	0
Refresh	0	0	0	1
Precharge	0	0	1	0
Activate Row	0	0	1	1
Write Column	0	1	0	0
Read Column	0	1	0	1
No Operation	0	1	1	1
Deselect	1	x	x	x

Table 2. SDRAM Commands.

Bus-Qualified Triggering

A performance mixed-signal oscilloscope provides many options to qualify signal capture using the state of command and control lines on the memory bus.

SDRAM memory commands are synchronized to the rising edge of the memory clock (CK). The four command signals are chip select (S0# or CS#), row address select (RAS#), column address select (CAS#) and write enable (WE#). The # symbol indicates these are active low signals (see Table 2). The verification of memory commands requires the MSO to probe five signals, CK, S0#, RAS#, CAS# and WE#, in addition to acquiring the appropriate data (DQ) and strobe (DQS) signals. In the MSO digital channel menu the five command signals – CK, S0#, RAS#, CAS# and WE# – are assigned to probe channels.

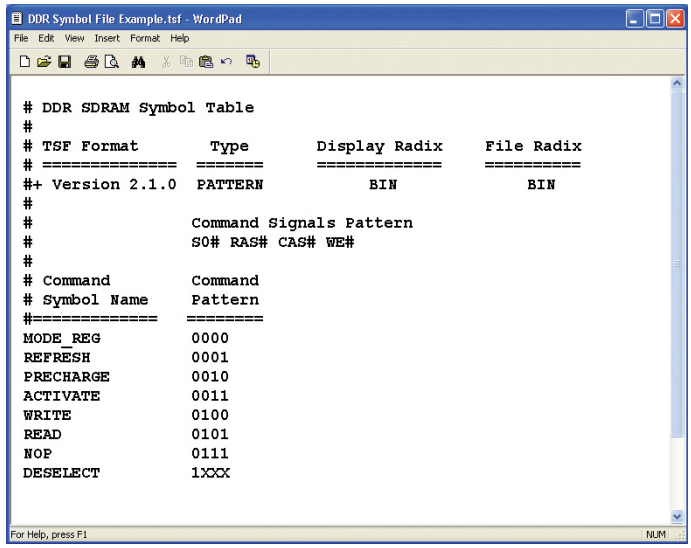


Figure 9. DDR Symbol File Example.

The Activate Row command is the first command of a write or read command sequence. To trigger the MSO on the Activate Row command, configure the MSO to trigger on a Command group equal to 0011. This is S0#=0, RAS#=0, CAS#=1 and WE#=1, as shown in Table 2.

Dealing with binary values like 0011 can be error prone. The MSO works with data in several formats: binary, hex, and symbolic. Pattern symbol files are used when a group of signals define a logical state such as the SDRAM command group. Based on the SDRAM command table, as shown in Table 2, a Tektronix Symbol File (.tfs) was created with Microsoft Notepad (see Figure 9).

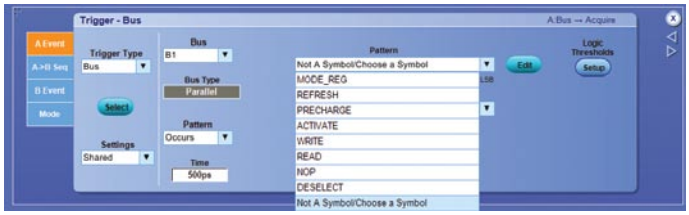


Figure 10. MSO70000 Symbol Trigger menu with DDR commands.

Figure 11. DDR3 Command Bus decoding on MSO70000.

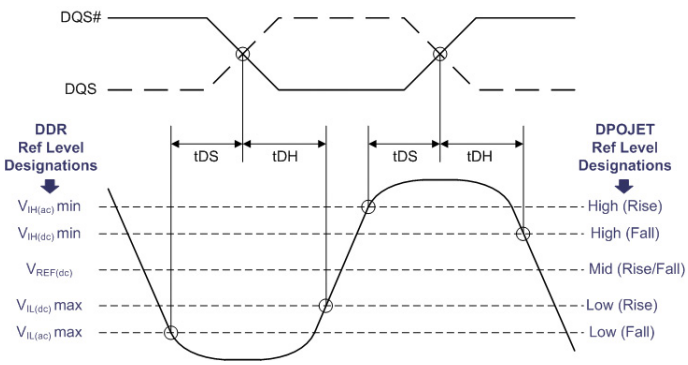


Figure 12. Measurement reference levels.

The MSO uses these pattern symbols when setting up the MSO to trigger on the Activate command (see Figure 10). To use pattern symbols in the MSO bus trigger menu, the Bus Radix is changed to Symbolic and the symbols become available for selection.

Performing JEDEC - Compliant Measurements

As mentioned earlier, the JEDEC specifications for each memory technology specify an array of conformance measurements specific to the technology. These include parameters such as clock jitter, setup and hold timing, transition voltages, signal overshoot & undershoot, slew rate and other electrical-quality tests. These specified tests are not only numerous but can also be complex to measure using general-purpose tools.

An example is measurement reference levels. JEDEC specifies certain voltage reference levels that must be used when making timing measurements. Figure 12 shows a graphic representation of the Vih and Vil levels (both AC and DC) that are used for timing measurements on data signals. Note that levels for rising and falling edges are defined differently.

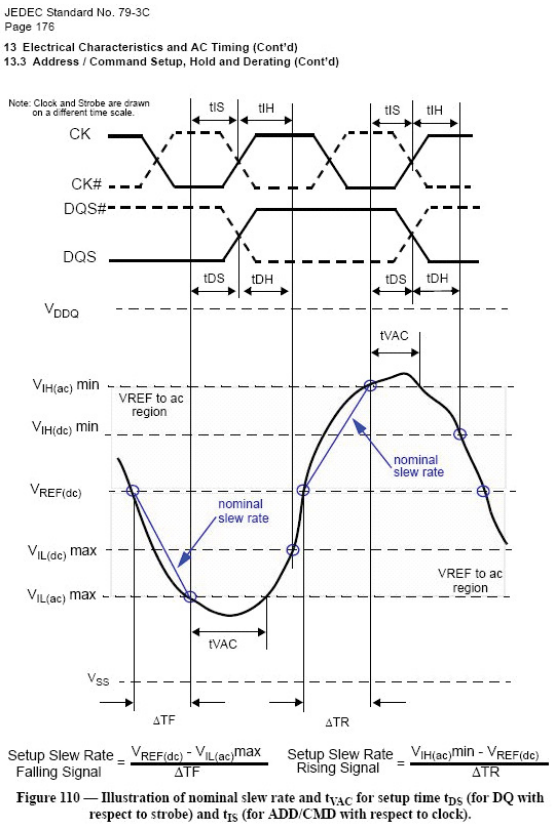


Figure 13. Slew Rate measurement - "Nominal" method for DDR3.

Another example is slew rate measurements. Slew rate must be measured on data, strobe, and control signals and is then used to calculate adjustments to the pass/fail limits for timing measurements such as Setup and Hold. But the details of how the slew rate measurement is performed varies depending on which signal is being measured. See Figure 13: the 'nominal' method is used for one set of measurements, while a different 'tangent' method must be used for another set.

Because of the complexity inherent in the JEDEC-specified measurement methods, reference levels, pass/fail limits, etc. it can be extremely valuable to have an application-specific measurement utility for DDR test. Using such a utility ensures that your measurements are configured properly and eliminates many hours of setup that would be required using general-purpose tools alone.

Figure 14. DDRA setup screen - Step 1.

DDR Analysis Software

Option DDRA for Tektronix real-time oscilloscopes (DPO/DSA70000 Series, MSO70000 Series, DPO7000 Series) is a software utility dedicated to automation and setup of measurements for testing DDR devices. The broad set of measurements available in DDRA all conform to the JEDEC specs, but the user also has the option to customize many settings for measurement tasks on non-standard devices or system implementations. This software option currently supports six different DDR technologies; DDR, DDR2, DDR3. LPDDR, LPDDR2, and GDDR3.

Option DDRA works in conjunction with two other software packages on the Tektronix oscilloscope; Advanced Search & Mark (Option ASM, described above) and DPOJET Jitter and Eye Diagram Analysis Tools. These three utilities work together to create a powerful, flexible yet easy-to-use suite for DDR testing and debug.

The menu interface for DDRA has five steps which guide the user through a selection process. Step one of the interface is shown in Figure 14. Here the user selects the DDR generation to be tested (DDR, DDR2, etc) and the speed grade of the memory. The drop-down selection box in this example shows all the commercially-available speed grades for DDR3 up to 1600 MT/s. In addition to the default choices, the user can enter a custom speed setting, making the software easily adaptable to future technology advances, overclocking applications, etc. Once the generation and data rate have been selected, DDRA automatically configures the proper voltage references for measurements. Here again there is a "User Defined" setting, allowing the user to override the JEDEC defaults and enter custom values for Vdd and Vref if desired.

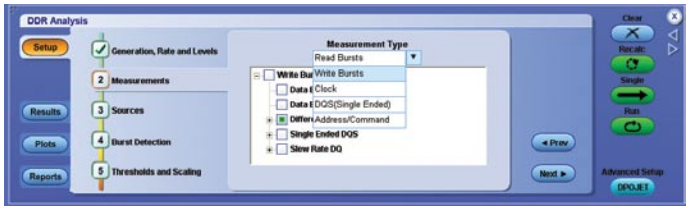


Figure 15. DDRA setup screen - Step 2 (measurement selection).

Step 2 allows the user to select which measurements to perform. The available measurements are grouped into drop-down menu selections according to which signals and probing connections are required. For example, measurements made on the Clock line are all grouped under a “Clock” drop-down menu. Read measurements, Write measurements and Address/Command measurements are similarly grouped into their own drop-down menus so that all measurements requiring a particular probing setup can be easily selected for a single test run.

The remaining steps 3, 4, and 5 in the DDRA menu interface guide you as to how the needed signals should be probed and offer additional opportunities for customizing or adjusting parameters such as measurement reference levels.

Once the setup is complete and the user selects <Run> (or <Single>) the oscilloscope will acquire the signals of interest, identify and mark data bursts if needed, and make the selected measurements. Using the default record length, the oscilloscope will typically acquire around 1000 unit intervals, taking measurements on all valid edges in the acquisition. When measuring data bursts, the software automatically generates an eye diagram showing both DQ and DQS overlaid to show relative timing. The DDRA “Results” panel shows all measurement results with their statistical population, spec limits, pass/fail results and other data. If desired, a printed report can be generated, with an option to also save the waveform data that was used to make the measurements.

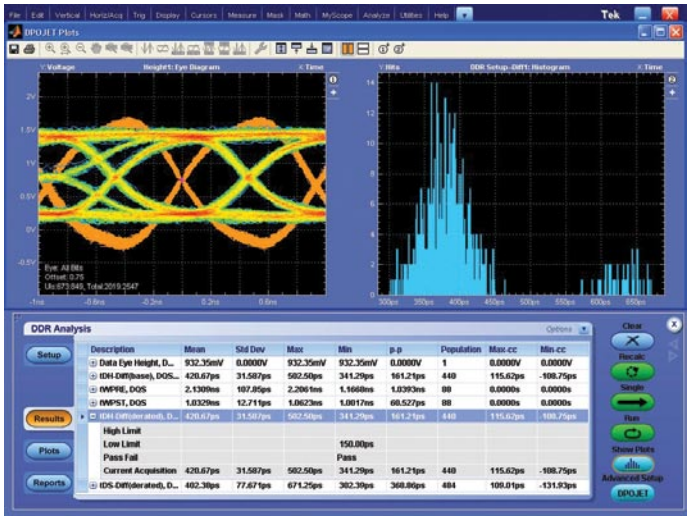


Figure 16. DDRA “Results” Screen showing two of the available plots.

Failure Analysis and Debug

Because all of the captured waveform data is available behind the measurement results, many options are available to the user beyond the results themselves. If a measurement fails the spec limits, it is possible to identify exactly where in the waveform record the failure occurred, then zoom in on the region of interest to investigate the exact signal details and characteristics at the time of failure. Several tools available in the software make it easy to analyze the captured data and to pinpoint regions of interest. For example, the Histogram plot shown in Figure 16, can be applied to any measurement of interest, showing worst-case measured values (in this example it has been applied to a Setup measurement.) Several other plot types are available. Tools such as “Cursor Sync” make it easy to link any data point in the plot back to its corresponding event in the original waveform record, making it simple to move back and forth between different views of the data for in-depth analysis.

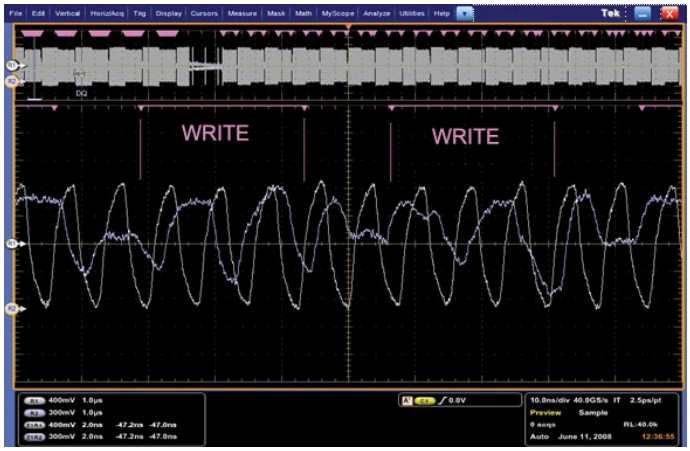


Figure 17. Back-to-back DDR3 Write operations.

Verifying Command and Protocol Operations

The protocol sequence for a SDRAM Write operation starts with the Activate command followed by one or more Write commands. The Activate command with its row and bank addresses opens a specific row in a specific bank for writes and reads. The Write command with its column and bank addresses opens a specific column in the opened row in a specific bank for writes. It would be a protocol error for the Write command to access a bank that has no open rows. After the Write command, the memory expects at a defined memory cycle that the memory controller hub will write data to it. The row needs to be closed or deactivated with a Precharge command when the writing is completed for the open row and another row is to be accessed. The simplest DDR2 SDRAM command protocol sequence is Activate, Write and Precharge. A consecutive write-to-write sequence is Activate, multiple Writes and Precharge. A write-to-read sequence is Activate, Write, Read, and Precharge. You can have any order of Writes and Reads on an open row. It would be a DDR2 DRAM protocol error if the memory controller hub sent two Write commands in a row without the Deselect command between them. The DDR2 DRAM will respond to the Write command by reading in data that is strobed by the memory controller hub.

Another key DRAM specification is the minimum tRP time after the Precharge command is sent and before the Activate command is sent to open a row. This can be easily verified by changing the MSO to trigger on the Precharge command and measuring the tRP time between the Precharge and Activate commands to the same bank.

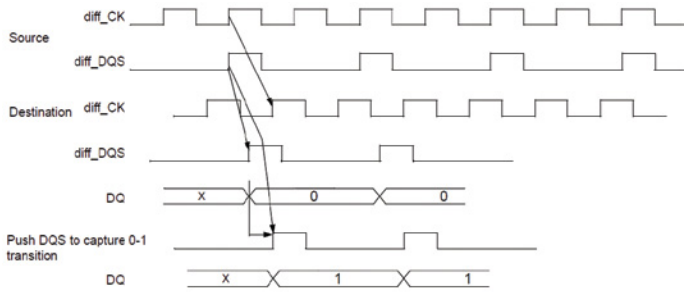


Figure 18. DDR3 Write leveling to deskew DQS and CK lines (source: JEDEC DDR3 SDRAM Standard, JESD79-3C).

The same protocol and timing verification techniques are applied to DDR3 DRAM read/write operations. Note however with DDR3 multiple back-to-back write operations are supported in the specification. When performing write burst isolation a continuous strobe may cause a write cycle to merge two back-to-back writes if care is not taken to match the termination logic of the strobe signal while analyzing bus traffic.

In addition to verifying complete read or write cycle operations other important verification tasks that should be performed include:

Basic functional testing

During prototype system initialization a quick check of clock, reset and PLL lines helps to identify any key issues that may propagate into other subsystems. Browser or handheld probes are useful in moving from point to point while checking “vital signs”.

Power management and other special operating modes

As the bus enters and exits power states certain lines may become inactive or turn back on. Careful attention is needed as these additional states add complexity in system interoperability. In Low Power DDR2 (LPDDR2), for example, devices incorporate advanced power management techniques such as Partial Array Self Refresh, allowing only necessary parts of the memory array to be used thus improving its efficiency and power consumption.

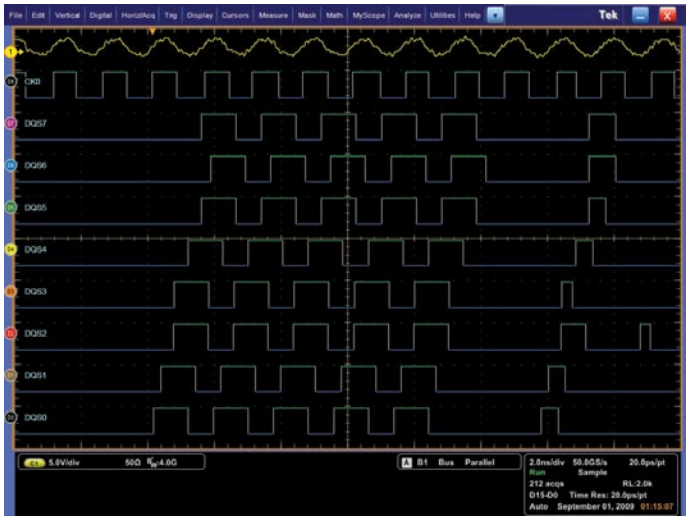


Figure 19. DQS0 – DQS7 skew relative clock during write leveling operation.

Figure 21. iCapture showing Chip Select line with analog and digital views.

Write/Read Leveling

Increasing bandwidth of source synchronous buses can be difficult if only data rate scaling is used. However higher bandwidths can be achieved with innovative physical layer design techniques. DDR3 supports a fly-by topology in which signals from the memory controller arrive at each memory component in a sequential manner, thus reducing loading and improving overall signal integrity. Because of the electrical delays between each component the memory controller needs to perform a delay calibration to realign the clock (CK) with the data strobe (DQS) for each component. Ensuring this operation functions properly helps reduce flight time skews between clock and strobe signals thus providing additional margin to the memory system.

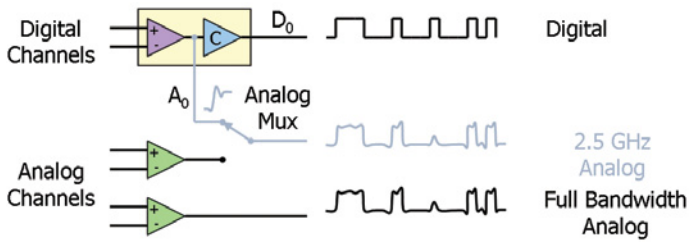


Figure 20. iCapture architecture.

DQ/DQS Margining

As mentioned earlier JEDEC outlines many measurements required for standards conformance. Silicon and component designers are looking beyond evaluation of basic parametric testing to understand and characterize the design over a range of process, voltage and temperature. A common example is to vary the Vref or Vdd lines and monitor data (DQ) and strobe (DQS) for noise immunity and sensitivity. This provides a higher confidence of the device working over a wider range of operating conditions.

Combining Digital and Analog Views

As discussed previously there are many options for accessing DDR signals, from interposers to solder-in probe tips. It's not uncommon to need to monitor many digital lines and then after uncovering a signal integrity issue add another probe to view the signal in its analog form. This is known as "double probing". It's an arrangement that can compromise the impedance environment of your signals. Using two probes at once will load down the signal, degrading the device's rise and fall times, amplitude, and noise performance.

With the iCapture feature the MSO70000 allows you to see time-correlated digital and analog behavior, without extra loading capacitance and setup time required for double-probing. Any of the sixteen digital channels can be "muxed" through the oscilloscope's analog signal path thereby providing a side by side digital and analog representation of the signal of interest. Figure 21 shows a simple illustration of verifying the Chip Select line on a GDDR5 design. This can be helpful in ensuring correct logic thresholds are used in sampling the digital data or verifying signal integrity with greater precision.

Summary

In this application note we've explored many of the challenges associated with DDR testing and have introduced tools needed for validation and debug of memory designs.
For more details about DDR testing visit the JEDEC page at http://www.jedec.org/ or http://www.memforum.org/index.asp. Here you will find detailed DDR specifications, white papers, and other support materials. Additional information about DDR testing can be found at www.tektronix.com/memory. This site includes extensive materials like application notes, webinars and recommended test equipment.

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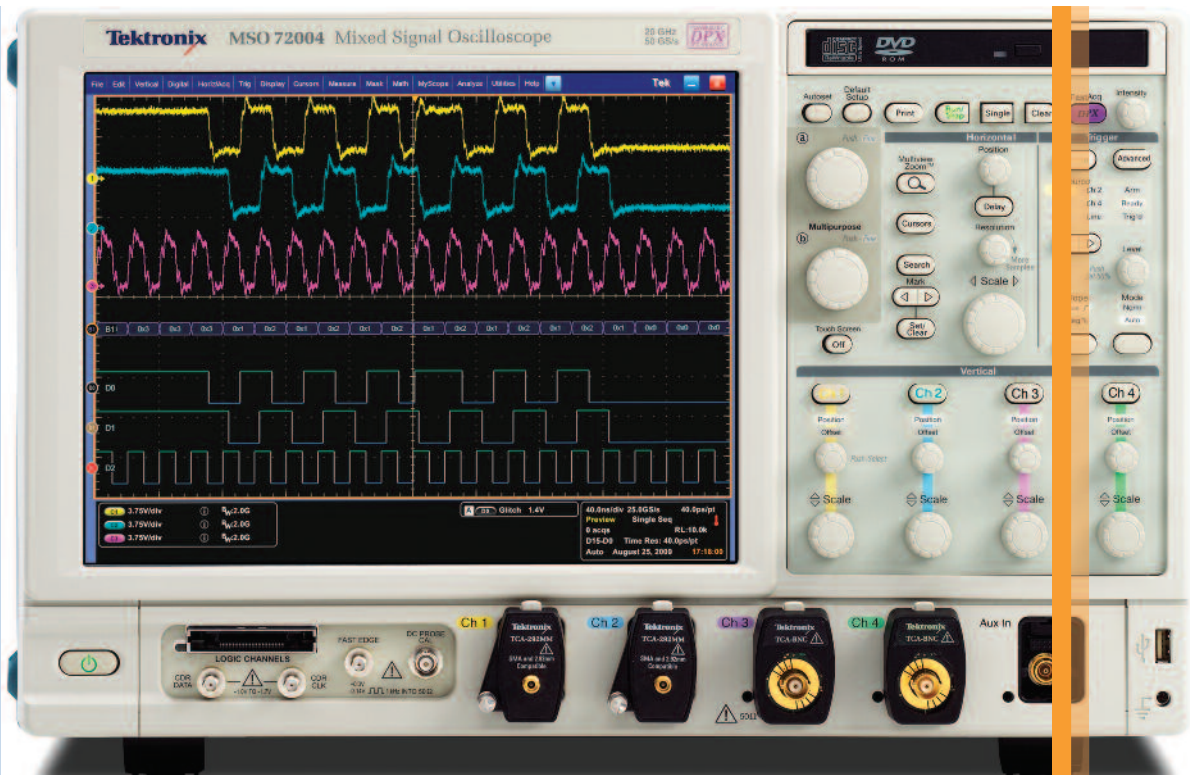

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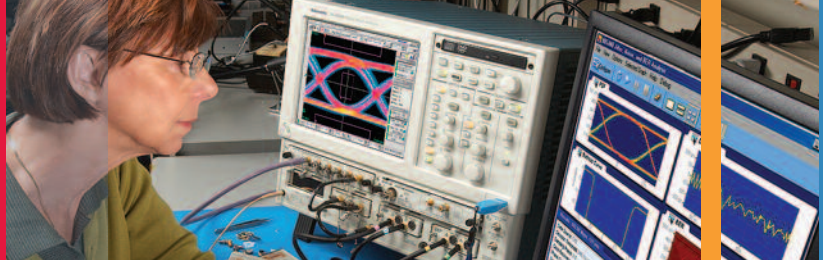


Powerful Analysis for Complex Digital Designs

Today's fast, complex digital designs require more PHY layer analysis than ever before. With the right oscilloscope, you can shave weeks from design verification cycles by performing measurement analysis right on the instrument. Tektronix performance oscilloscopes contain the analysis capability needed to speed up critical serial, mixed signal and RF debug and design verification.

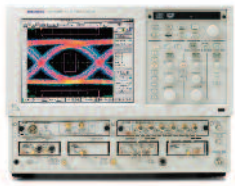
Tektronix performance oscilloscopes have access to more than 30 different debug and analysis packages, from the popular DPOJET jitter analysis tool to SignalVu,™ a comprehensive RF signal analyzer suite. For 3rd Generation Serial Designs with bandwidths from 8 up to 80+ GHz, Tektronix performance oscilloscopes provide critical capabilities for the most advanced electronic designs. Using patented Silicon Germanium IC technology; Tektronix delivers the industry's best signal fidelity and the lowest noise floor. This gives you the measurement accuracy to perform critical rise-time, jitter and noise measurements with confidence.

Performance Oscilloscope Product Selection

DPO7000

DPO/DSA70000B

MSO70000



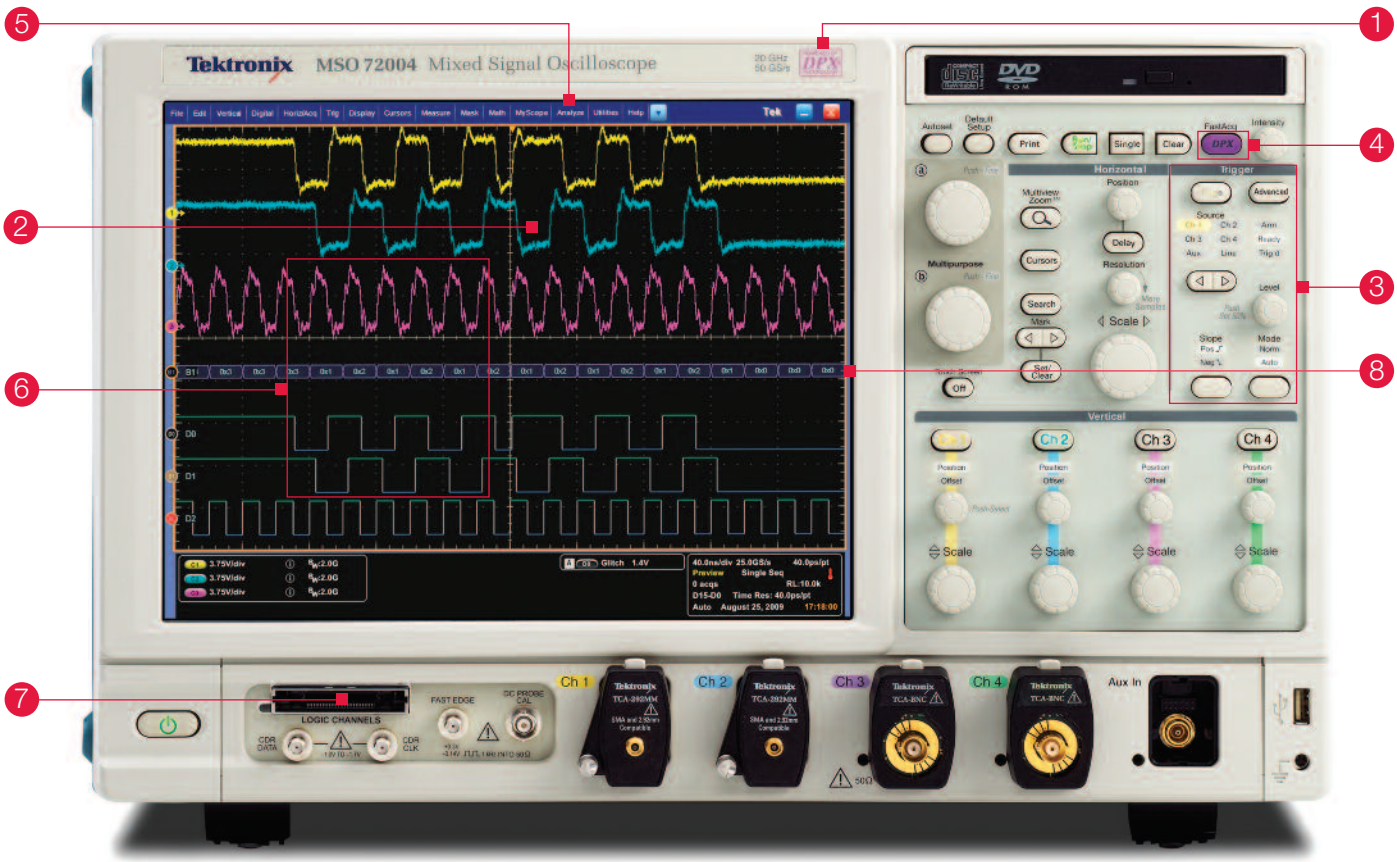
DSA8200

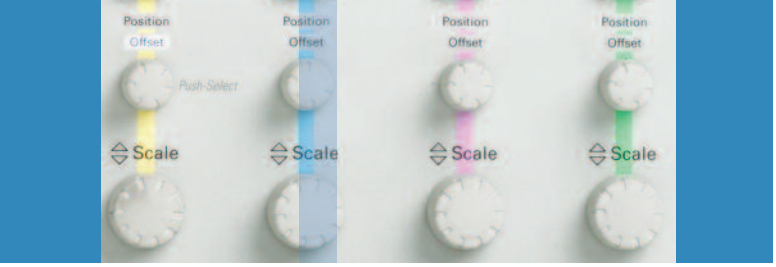
	DPO7000	DPO/DSA70000B	MSO70000	DSA8200
Channels	4	4	4 + 16 Logic Channels	Up to 8
Bandwidth	500 MHz to 3.5 GHz	4 to 20 GHz	4 to 20 GHz	DC - 80+ GHz
Rise Time 20% to 80% Typical	95 ps to 310 ps	14 ps to 68 ps	14 ps to 68 ps	5 ps
Sample Rate	Up to 40 GS/s	Up to 50 GS/s	Up to 50 GS/s Analog Channels 12.5 GS/s Logic Channels	200 kS/s (sequential)
Maximum Record Length	Up to 400 M points	Up to 250 M points	Up to 250 M points	—
Maximum Waveform Capture Rate	> 250,000 wfm/s	> 300,000 wfm/s	> 300,000 wfm/s	N/A for sampling oscilloscopes
Digital Timing Resolution	N/A	N/A	80 psec	N/A
Trigger Types	Over 1400 Combinations of A/B triggers (e.g., Glitch, Pulse Width, Timeout, Transition, Communications). Common serial bus triggers including: I^2C, SPI, RS232, UART, CAN. Video Sync Pulse.	5 Gb/sec Serial Pattern and over 1400 Combinations of A/B triggers (e.g., Glitch, Pulse Width, Timeout, Transition, Communications). Common serial bus triggers including: I^2C, SPI, RS232, UART, CAN.	Bus Cycle, Logic (Pattern State/Setup & Hold), 5 Gb/sec Serial Pattern and over 1400 Combinations of A/B triggers (e.g., Glitch, Pulse Width, Timeout, Transition, Communications). Common serial bus triggers including; I^2C, SPI, RS232, UART, CAN.	Edges, Internal Clock, Clock Recovery
Application Software	Windows operating system and over 20 different debug and analysis packages including: ■ Jitter and Timing Analysis ■ Advanced Search and Mark ■ Debugging and Compliance Testing of 1st and 2nd Generation Serial Data Designs ■ Power Measurements and Analysis ■ Spectral Analysis	Windows operating system and over 30 different debug and analysis packages including: ■ Jitter and Timing Analysis ■ Advanced Search and Mark ■ Debugging and Compliance Testing of 1st, 2nd and 3rd Generation Serial Data Designs ■ De-Embedding, Equalization and Serial Data Link Analysis (SDLA) ■ Power Measurements and Analysis ■ Spectral Analysis ■ Debugging and Compliance Testing of WiMedia UWB Standards	Windows operating system and over 30 different debug and analysis packages including: ■ Jitter and Timing Analysis ■ Advanced Search and Mark ■ Debugging and Compliance Testing of 1st, 2nd and 3rd Generation Serial Data Designs ■ De-Embedding, Equalization and Serial Data Link Analysis (SDLA) ■ I^2C and SPI Trigger and Decode ■ Power Measurements and Analysis ■ Spectral Analysis ■ Debugging and Compliance Testing of WiMedia UWB Standards	Windows operating system, optical and electrical modules and analysis software including: ■ Advanced, Jitter, Noise and BER Analysis ■ ITU/ANSI/IEEE/SONET/SDH Conformance ■ High-Performance True Differential TDR Measurements ■ Impedance Characteristics and Network Analysis for Serial Data Applications Including S-parameters ■ De-Embedding, Equalization and Serial Data Link Analysis (SDLA) ■ Channel & Eye diagram Simulation and Measurement-based SPICE Modeling

* Optional

Achieve Greater Design Insight

Featured Performance Product: MSO70000 Mixed Signal Oscilloscope





1 Uncompromised Analog and Digital Acquisition Specs

Don't miss critical signal events with high sample rate across all channels and very long record length. Tektronix Performance Mixed Signal Oscilloscopes ensure that you capture important analog and digital signal details of interest with the deepest possible levels of resolution and time interval detail to meet your design goals with confidence.

2 Integrated Analog and Digital Visibility

Time-correlated analog, digital and bus displays enable a broad level of system design visibility providing better debug of correlated events. Perform embedded design validation on systems featuring high speed memory (DDR), FPGA's.

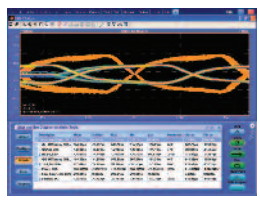
3 Pinpoint and Logic/Bus Triggering

Speed up debugging with a comprehensive trigger tool that leads the industry in usability and depth of signal event capture behavior. Capture events of interest using a broad array of triggers matched to your signal type. If searching for a bus-related behavior, trigger on a defined bus cycle type. For a specific pulse width, trigger on a pulse down to 400 picoseconds. Find what you're looking for...**fast!**

4 FastAcq, Powered By DPX®

Keep your design project on track by finding problems fast with Tektronix proprietary acquisition technology. Discover infrequent events and "see a world that others don't" using the power of DPX, an industry award-winning capability that completely changes the paradigm of debugging.

5 Full Suite of 30+ Serial Compliance and Analysis Options

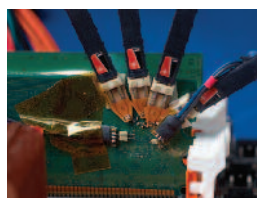


Simplify compliance verification and debugging of communications system designs such as Ethernet and USB. Fix timing issues fast with industry favorite DPOJET Timing and Jitter Analysis.

6 iCapture™ for Deeper Digital Signal Insight

Acquire and view a signal in the digital or analog domains with a single probe connection using Tektronix' unique iCapture technology. Built into the MSO70000's acquisition system; iCapture enables a new paradigm for digital signal verification with switchable analog views on any of the 16 logic channels.

7 Accurate Probing and Versatile Connectivity



Keep your design moving in the right direction with perfectly matched Tektronix analog and digital (Logic) probes that connect to virtually any board or interconnect environment. For example, using the P6780 Logic Probes, you can acquire high speed, differential or signal ended buses with minimal probe loading.

8 Serial Protocol Decode and Search

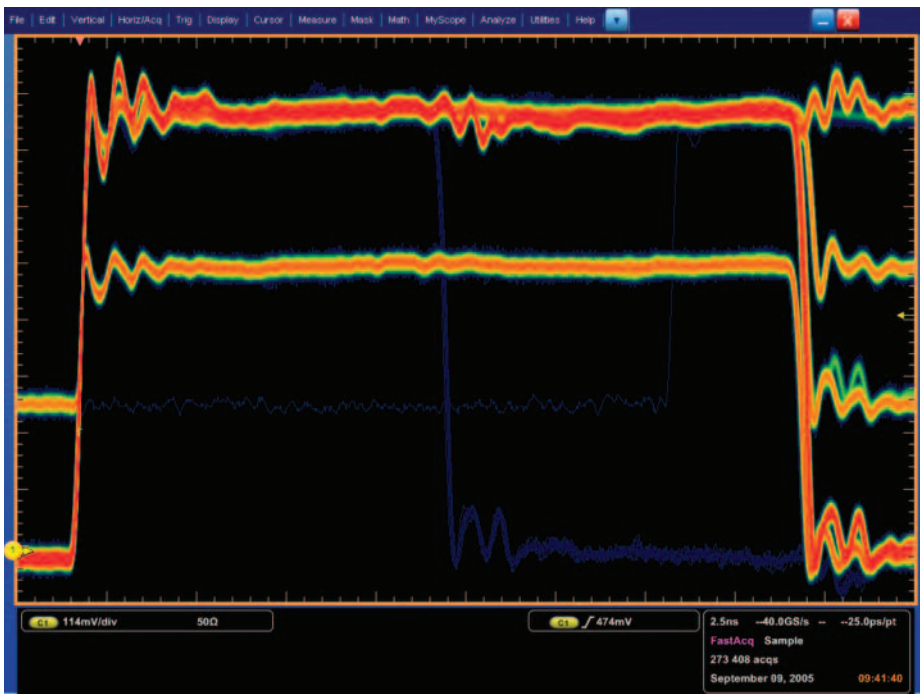
Speed up communications bus debugging by viewing incoming signals in decoded bus symbol formats alongside analog waveform displays. Optional support for popular busses including I^2C, SPI, PCI Express, Serial ATA and others.

Discover

Don’t Miss Important Signal Behavior

Identifying signal fidelity issues early on is critical in any high-speed communications system design. Tektronix Performance Oscilloscope contain the powerful acquisition and display technology to enable accurate representation, capture and display of all signal events of interest to you.

Equipped with ground breaking Silicon Germanium IC Technology that enables uncompromised bandwidth, sample rate, and record length, signal data is fully represented for your analysis. Tektronix’ patented DPX® acquisition technology enables identification in real-time of infrequent events to rapidly solve debugging challenges. When evaluating critical signal behavior, leave nothing to chance with Tektronix Performance Oscilloscope.

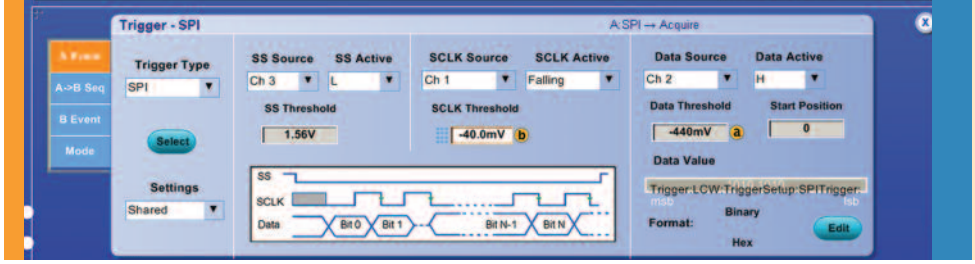


Digital Phosphor Technology FastAcq and DPX®

More than just color-grading, FastAcq's proprietary DPX® acquisition technology captures signals at more than 300,000 waveforms per second on all four channels simultaneously. This dramatically increases the probability of discovering infrequent events, as illustrated in the photo on the left where the faint blue trace might have been completely missed on another vendor's oscilloscope. Some oscilloscope vendors claim high waveform capture rates for short bursts of time, but only Tektronix DPO7000, DPO/DSA70000B and MSO70000 Series oscilloscopes can deliver these fast capture rates on a sustained basis. Reduce your debug time by minutes, hours or even days by quickly revealing the nature of potential faults.

Time-Correlated Analog/ Digital Display

The large display of the MSO70000 Series enables a robust view of up to 20 channels of captured signal content with a single trigger event. View time coincident data in multiple domains like control and data lines to better understand system integration issues on your design with precise accuracy. Develop conditional serial bus tests to determine viability in complex mixed signal designs.

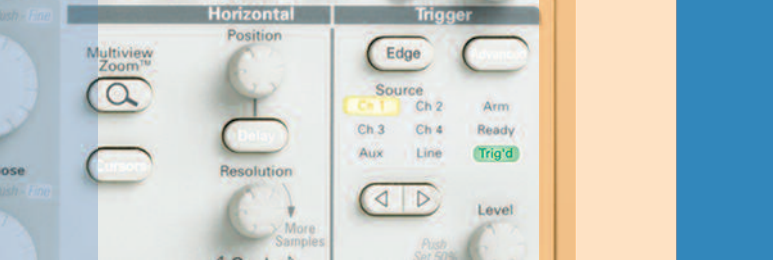


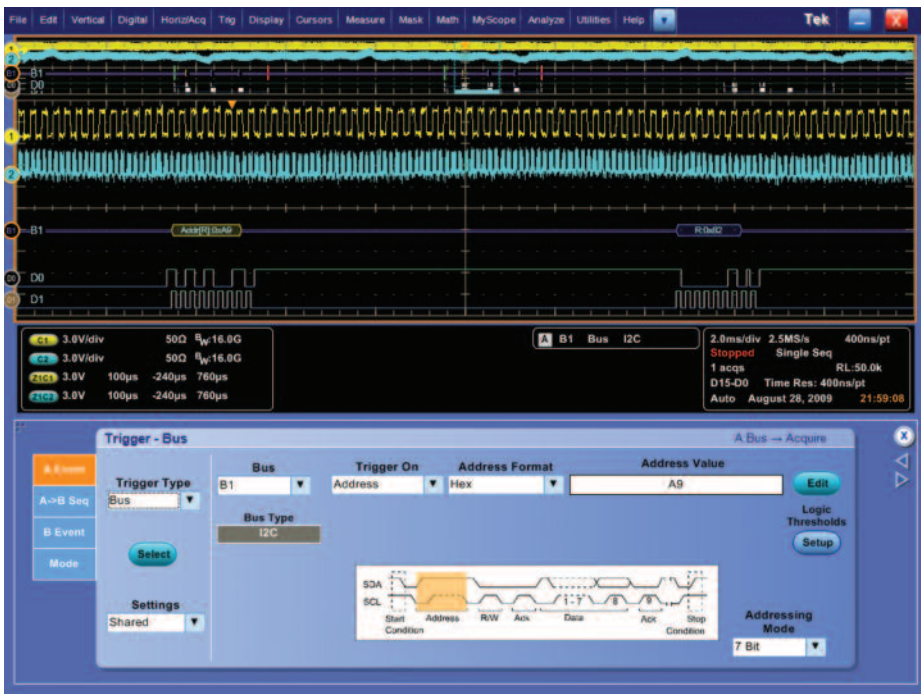
Capture

Get to the Source of the Issue Faster

High-speed signals with long pattern lengths can be challenging to debug. Having a comprehensive triggering system takes the complexity out of event identification and frees up more time for your design analysis tasks.

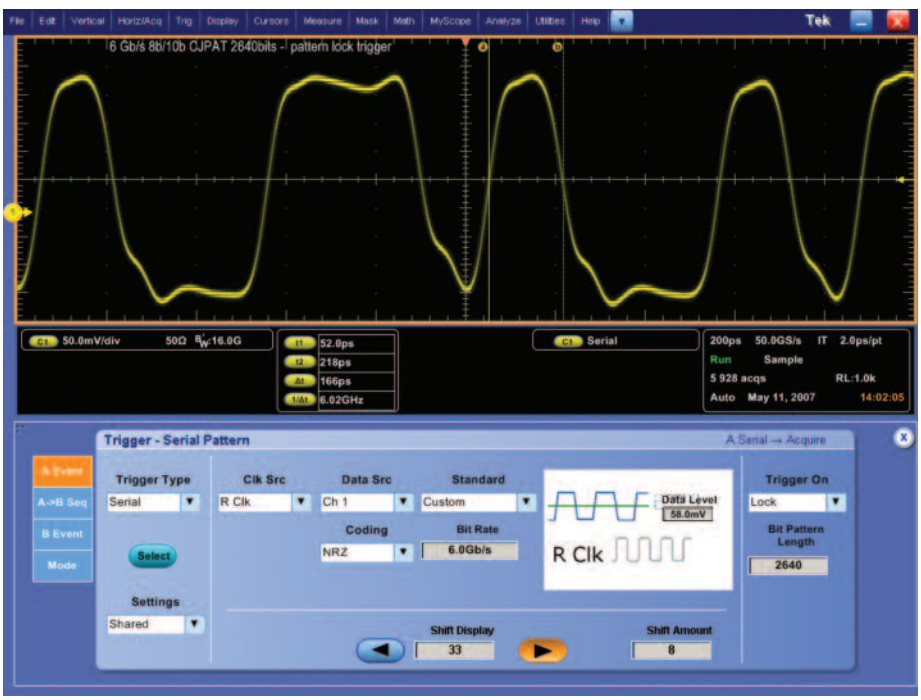
Enabled by a ground-breaking acquisition system architecture, Tektronix Performance Oscilloscopes come equipped with the industry's fastest and most comprehensive triggering systems. With over 1400 event combinations, you can setup trigger conditions that get to the source of any complex signal event. The Serial Pattern trigger capability built into the DSA70000B Series greatly simplifies capture of protocol level detail on your designs, up to a fast 5 Gb/sec data rate. Logic-qualified triggers are available on the MSO70000 Series to capture events that only appear during specific bus cycles, speeding up verification of complex signaling architectures like PCI Express, DDR Memory.





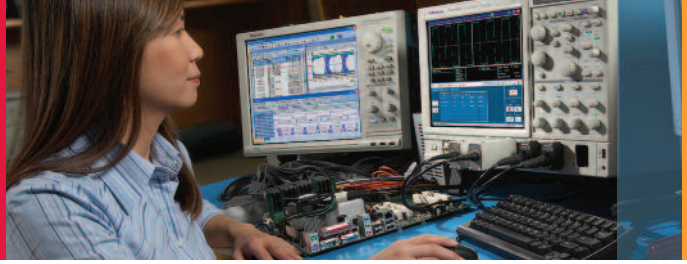
Advanced Pinpoint® Triggering

The ability to trigger an oscilloscope on events of interest is paramount when debugging and verifying complex signals. Whether you're trying to find a problem signal, or isolate a specific section of a complex signal, Tektronix Pinpoint® triggering provides the solution. It has an extremely high trigger sensitivity, very low trigger jitter and the ability to capture narrow glitches. Pinpoint triggering delivers more than 1400 trigger-setting combinations, all at full performance, so events in the most complex signals can be captured. Tektronix also offers Serial Pattern and Pattern Lock triggering up to 5Gb/s. The MSO70000 Series provides Logic-qualified and bus-specific triggers like I^2C (as shown on left) for mixed signal designs.



5Gb/s Protocol and Serial Pattern Triggering

To debug serial architectures with data rates up to 5Gb/s and correlate events across physical and link layers, use the DSA70000B's Serial Pattern triggering with built-in hardware PLL-based clock recovery for NRZ and 8b/10b serial data streams. Recover the clock signal, identify transitions and set the desired encoded words for the serial pattern trigger to capture. Pattern Lock triggering adds an extra dimension by enabling synchronized acquisitions. This allows you to remove random jitter from long serial data patterns, investigate specific bit transitions and use mask testing for averaging purposes.

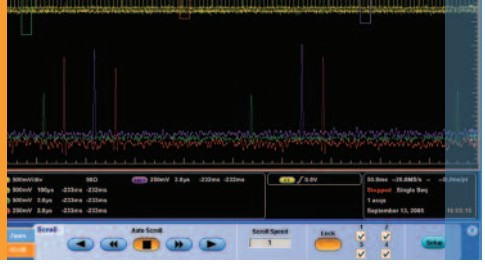


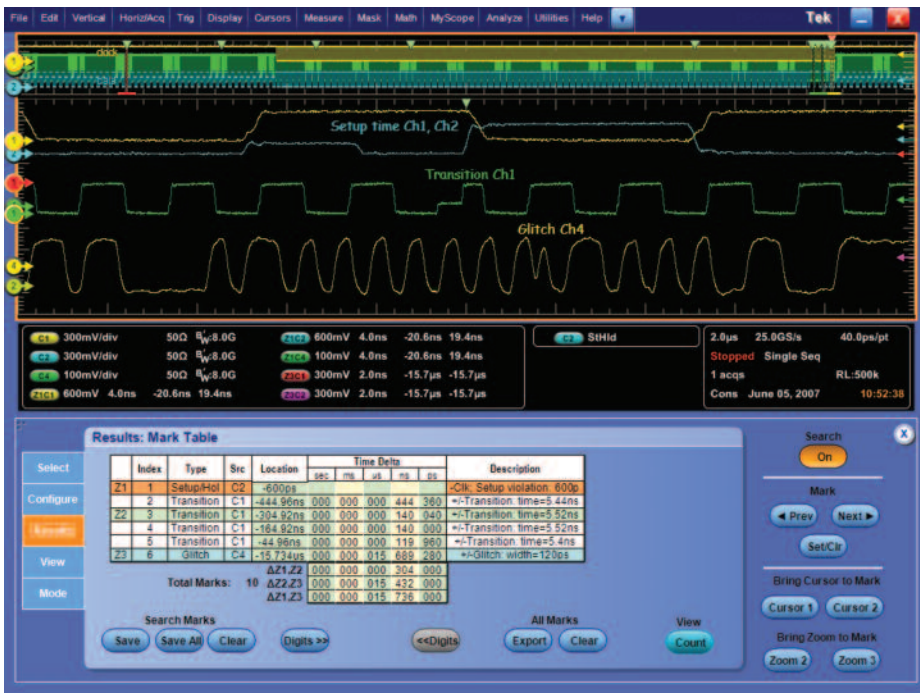
Search

Navigate Quickly Through Millions of Unit Intervals

High-speed digital signals that require timing verification for sources of jitter often mean capturing of millions of unit intervals (UI's). With Tektronix Performance Oscilloscopes, you have very long record length for seamless data capture, and intuitive, easy to use zoom, search, and mark tools that enable finding specific events of interest.

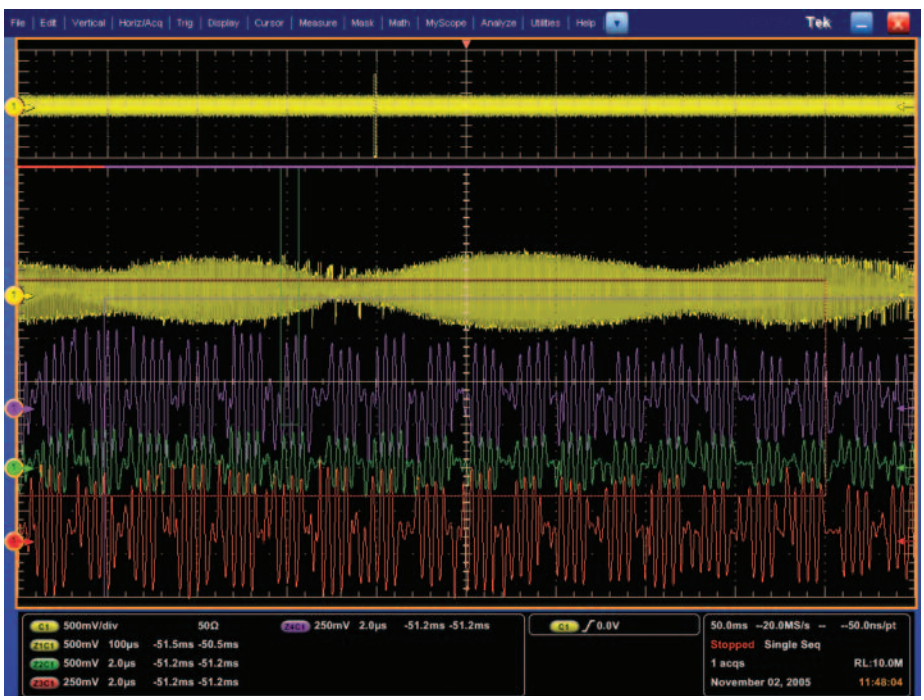
When coupled with Tektronix' industry leading Pinpoint Triggering System, and the comprehensive jitter analysis features of DPOJET, Tektronix Performance Oscilloscopes are the ideal tool for capturing long records of high speed digital signal waveform data and debugging it for sources of timing errors or jitter.





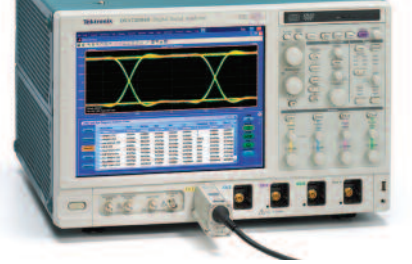
Search and Mark Events Within Long Records

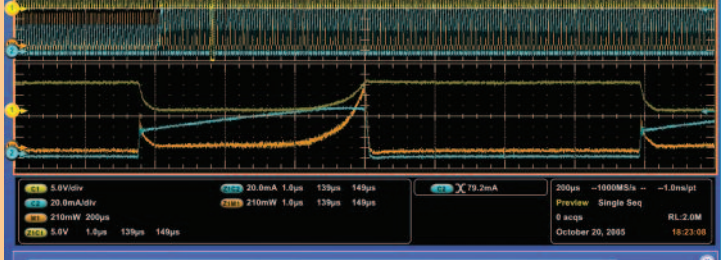
Finding important events such as fast or slow transitions, setup and hold violations, or logic patterns within a long-record capture is made easy with Advanced Search and Mark. It features unprecedented flexibility and increased precision for locating signal features of interest. Advanced Search and Mark is closely coupled with the Pinpoint trigger system and extends signal-shape discrimination features across live channels, stored data and math waveforms.



Multi-View Zoom

Many high performance designs require validation involving multiple channels of time-correlated data across many UI's. To simplify the tasks of comparing multiple waveforms and examining long records in successive levels of detail, Multi-View Zoom provides as many as four zoom "regions" which can be defined and displayed simultaneously to reveal signal behavior at different resolutions.





Analyze

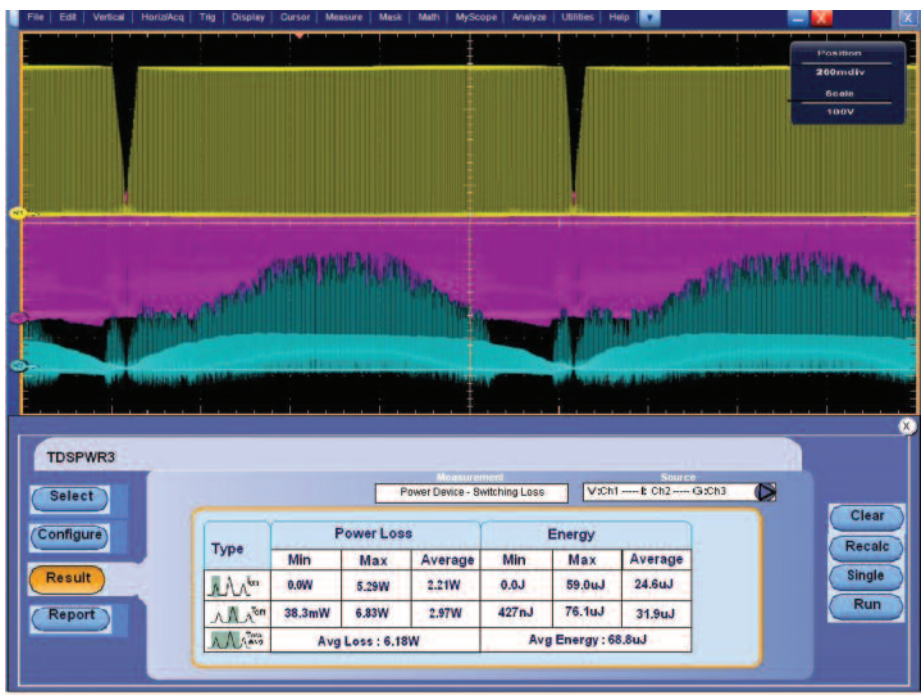
Accelerate Your Design Validation and Standards Compliance Efforts

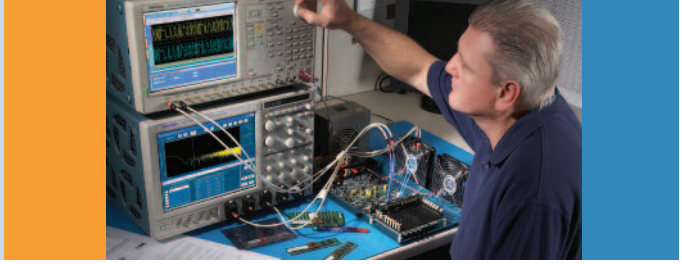
Sometimes the difference between failure and success lies in the availability of the right tools. Tektronix offers dedicated analysis solutions for many of today's and tomorrow's measurement challenges. With more than 30 different software packages – from technology-specific measurement and compliance software to application-based solutions for jitter and timing analysis, channel emulation and equalization – you can analyze a wide variety of your most challenging system designs.

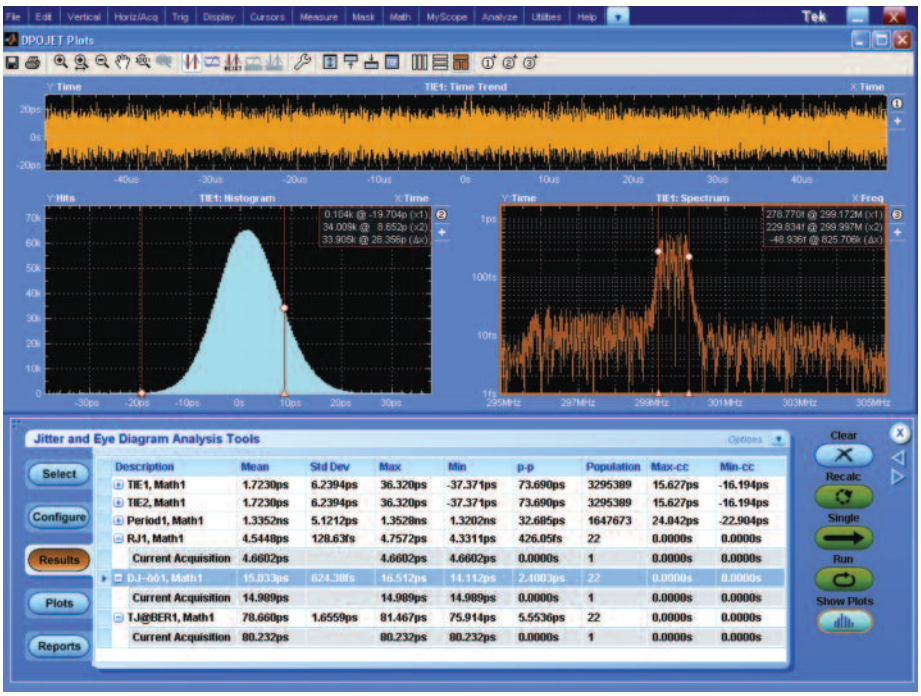
The following software applications represent a selection only. For more information, please contact your local sales representative or visit www.tektronix.com.

Switched Mode Power Supply Analysis

Quickly and accurately analyze your power supply with automated measurements for power quality, harmonics, switching loss, safe operating area, modulation, ripple, and slew rate. This analysis tool has intuitive setups enabling you to perform consistent measurements. The reporting capability is ideal for vendor part qualification, workgroup sharing or IEEE certification.

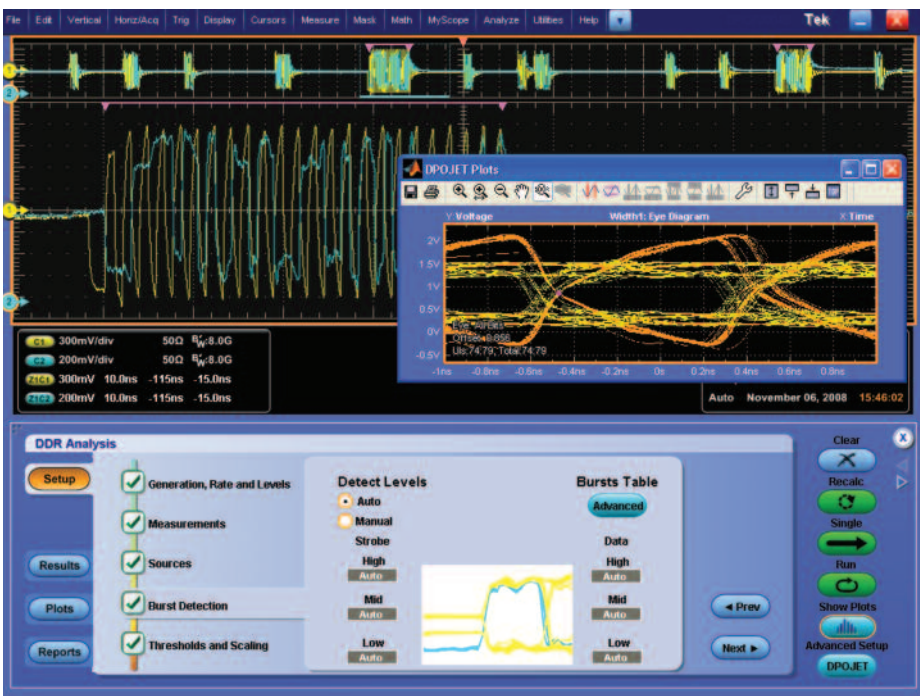






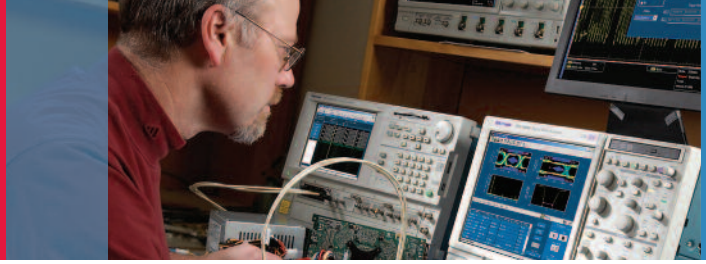
DPOJET Jitter and Eye Diagram Analysis

Simplify the identification of high-speed timing issues, jitter and their related sources with DPOJET software. This comprehensive analysis suite provides you with trending data and graphs, spectral content and multi-plot displays. There are also 99 different measurements available; everything from jitter separation to Pre-Emphasis signal identification. DPOJET provides the greatest insight on timing and jitter available for real-time oscilloscopes on the market today.



DDR Memory Bus Analysis

Automatically identify DDR1, LP-DDR1, DDR2, DDR3 and GDDR3 Reads and Writes to clearly see how analog anomalies are affecting your DDR/Memory design. Verify conformance to JEDEC standards like JESD79-3C using this powerful toolset. DDR Analysis Software, when installed on Tektronix Performance Oscilloscopes containing DPOJET and DPX® technology; provides the fastest solution in the industry for debugging complex memory signaling issues.

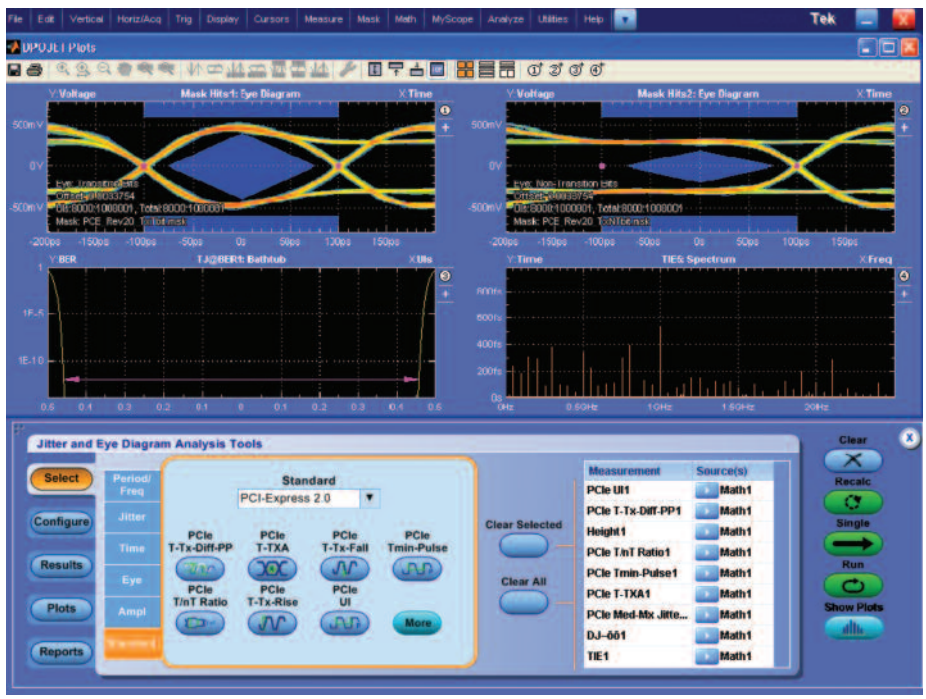


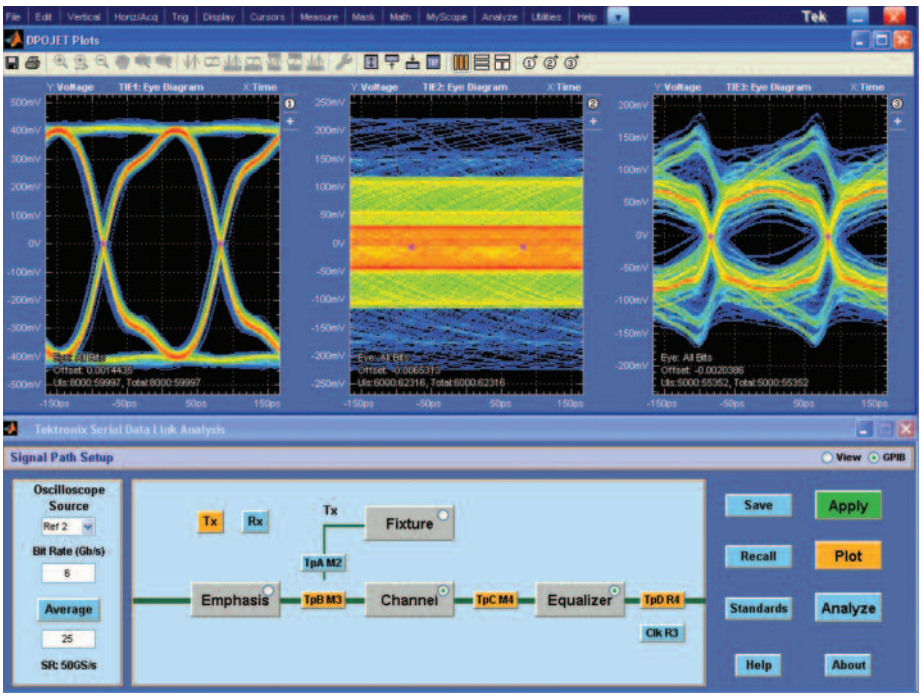
Analyze

The following software applications represent a selection only. For more information, please contact your local sales representative or visit www.tektronix.com.

Serial Data Standards Analysis

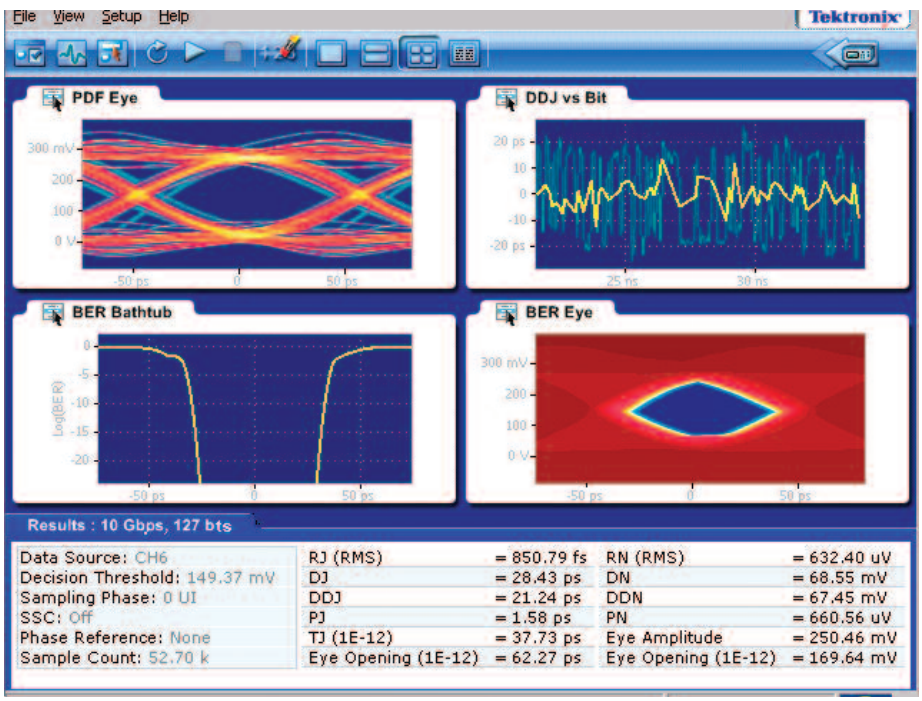
Analyze the performance of your PCI-Express design, get compliance test results on USB transmitter performance tied to USB-IF standards or verify compliance to the latest HDMI CTS specs. Tektronix enables tests that are tightly aligned to specific PHY layer test requirements for the most common Serial Standards; from HDMI and DisplayPort to USB, PCI Express and Serial ATA.





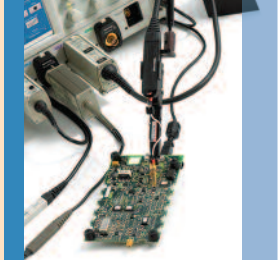
Serial Data Link Analysis

Gain insight into serial data system-wide performance with this powerful tool. Using SDLA, you can perform real-time cause/effect jitter measurements by emulating the serial data channel from its S-parameters, de-embedding the signal impact of fixturing, adding or removing pre/de-emphasis and emulating FFE and DFE equalization effects.



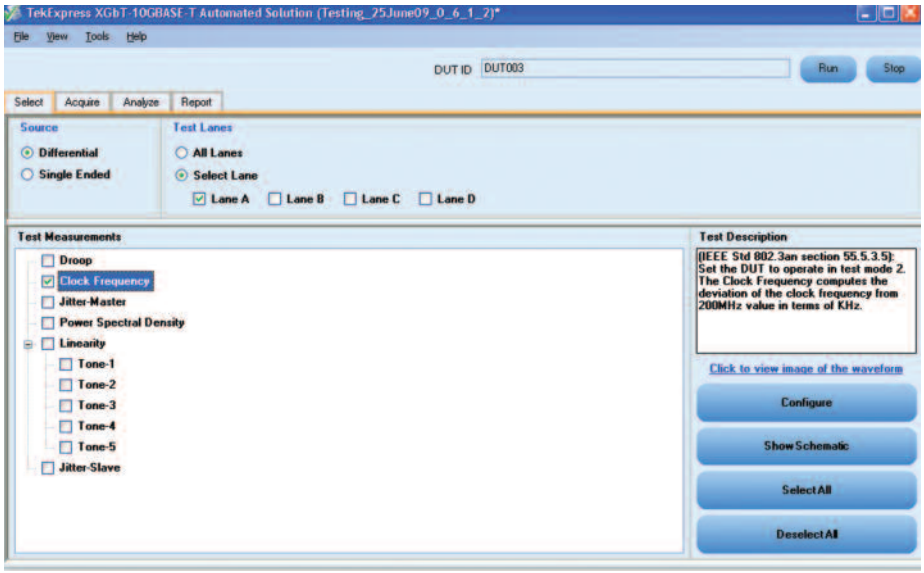
Jitter, Noise, BER and Serial Data Link Analysis

Perform highly accurate BER estimation based on both jitter and noise impairments enabling robust insight beyond simple jitter-based bathtub estimation. Available as an option on DSA8200 Series Sampling Oscilloscopes, the jitter and noise impairment measurements can be combined with link analysis tools to emulate channel and equalization effects, providing you with a level of analysis unavailable on a conventional Bit Error Rate Tester.



Ethernet Compliance Testing

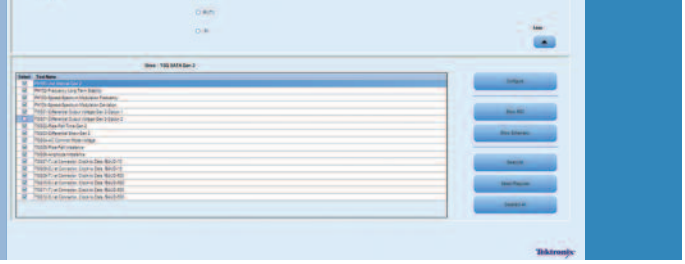
Comprehensive PHY layer test support for Ethernet variants from 10BASE-T to 10GBASE-T with a comprehensive, integrated Ethernet tool set. Analog verification, device characterization and automated compliance solutions are all included.

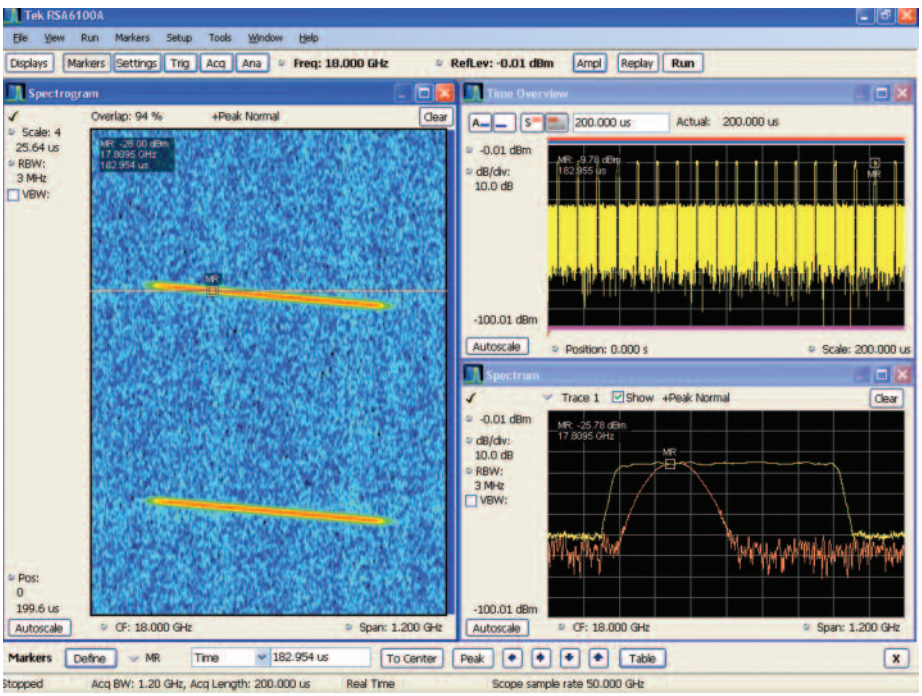


Parallel, I²C & SPI Capture and Decode*

View the control state of your device under test while debugging other signals on your design. Capture and view common command & control buses alongside other time-correlated events on one of the MSO70000's four analog channels.

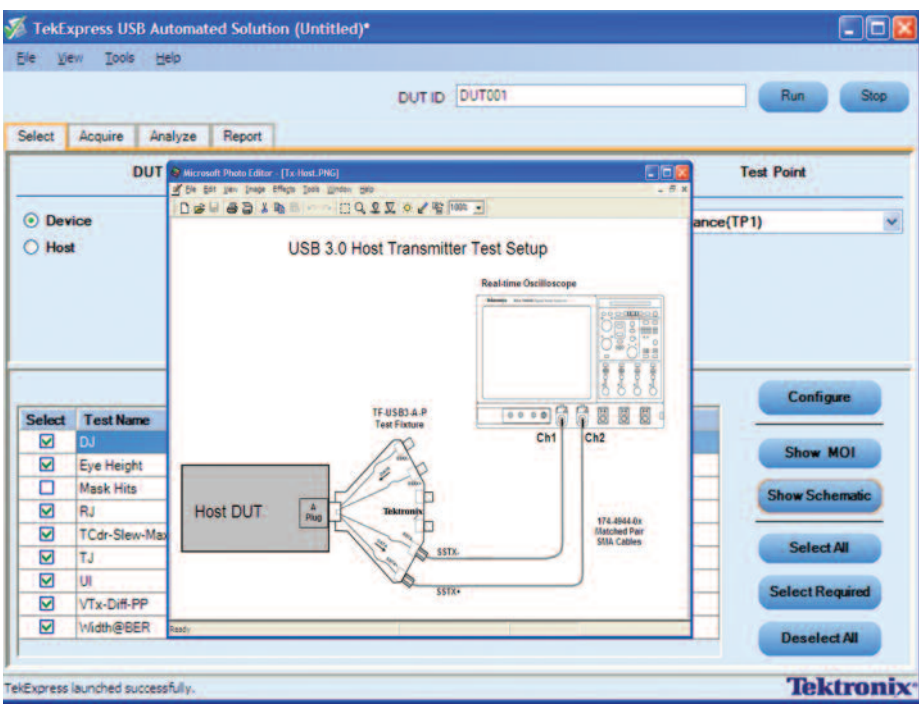
*Note: Available on MSO70000 Series only.





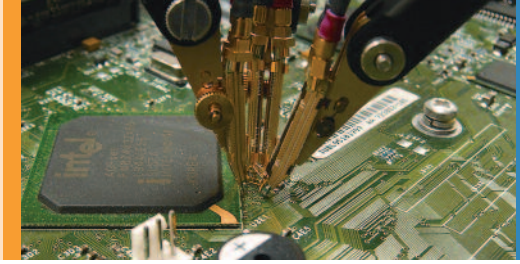
SignalVu™ Vector Signal Analysis

Easily characterize wideband spectral events and verify designs such as wideband radar, high data rate satellite links or frequency-hopping radios. SignalVu combines the functionality of a vector signal analyzer, a spectrum analyzer and triggering capabilities of a Tektronix oscilloscope in a single package.



TekExpress™ Automated Compliance Test Software

Reduce your compliance test time by 70% with the automation of all required testing suites provided by TekExpress software. TekExpress provides auto-recognition of required test equipment, precise DUT/Host control, while supporting all generations of SATA, DisplayPort, Ethernet and Superspeed USB (3.0) defined test suites.



Connectivity

Measurement Accuracy Begins at the Probe Tip

No oscilloscope is complete without the ability to capture signals accurately. Whether it be an optical front end for high-speed Ethernet or a properly configured probing system for differential signal captures on a PCI Express lane, Tektronix offers the industry's widest range of connectivity solutions for any measurement challenge. From high-speed differential probes for the most demanding Serial Data Compliance measurements, to a broad selection of sturdy active and passive probes for accurate mixed signal capture, Tektronix has your needs covered.

Tektronix has over 100 different probes available.

Active Probes

TAP2500

Differential Probes

P7516

Passive Probes

P2220

Current Probes

TCP0030

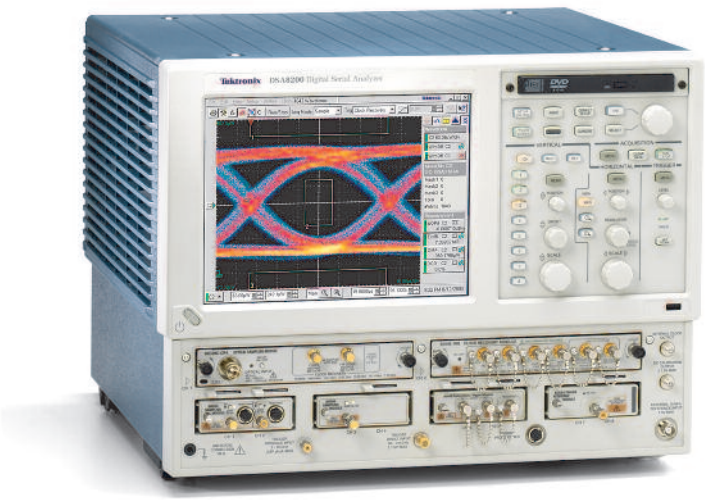
Differential Logic Probes

P6780 (works with MSO70000 Series Oscilloscopes only.)

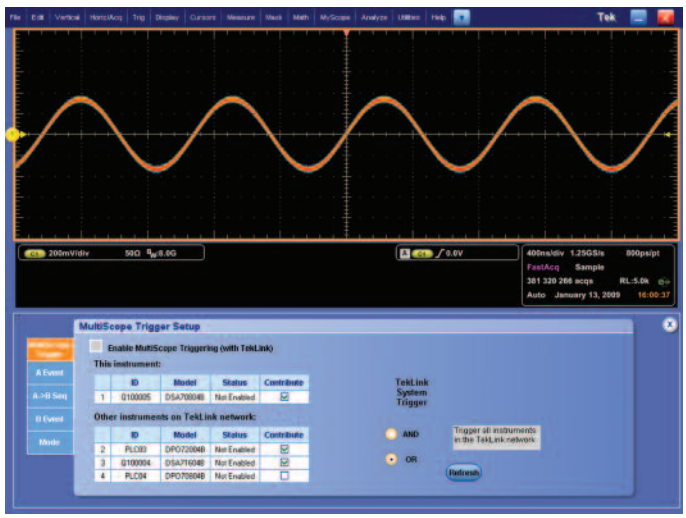
High Voltage Probes

P6015A

For a specific fit to any application or Tektronix oscilloscope, visit the Interactive Probe Selector at www.tektronix.com/probes



DSA8200 with Optical Inputs



TekLink

Optical Signal Connectivity

The versatile, modular architecture of the DSA8200 supports a large and growing family of plug-ins, including Tektronix optical modules which provide complete optical signal connectivity test solutions with superior system fidelity from 125 Mb/s to 43 Gb/s and beyond, covering a range of wavelengths for both single and multi-mode fibers.

Time-Aligned Instrument Control with TekLink™

TekLink is a high-speed instrument control network which enables multiple Tektronix instruments to be controlled on a time-aligned basis for large multi-channel acquisitions or in systems requiring synchronized stimulus & analysis. For example, when >4 channels of acquisition are needed on a single trigger event, TekLink will ensure alignment across multiple DPO/DSA70000B & MSO70000 Series Oscilloscopes. Ideal for manufacturing test or key research projects.

Maintain Your Oscilloscope at Peak Performance

The DPO/DSA/MSO Performance Oscilloscopes and Probes come standard with a 1-year warranty covering all parts and labor.

Tektronix offers a range of repair and calibration plans to extend your coverage and keep your instrument operating at optimal performance.

Repair Service Extended Coverage

- Save money with multi-year coverage
- Priority service
- Covers equipment, parts, labor and transportation
- Applicable software, safety and reliability updates

Calibration Service Coverage

- Accredited calibration
- Traceable calibration
- Functional verification
- Applicable software, safety and reliability updates
- Calibration records retention

Multi-Vendor Calibration Service

- Single point of contact for all of your calibration needs
- Simplify your operations and reduce administrative costs
- On-site delivery for convenience and reduced downtime

Contact Tektronix:

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