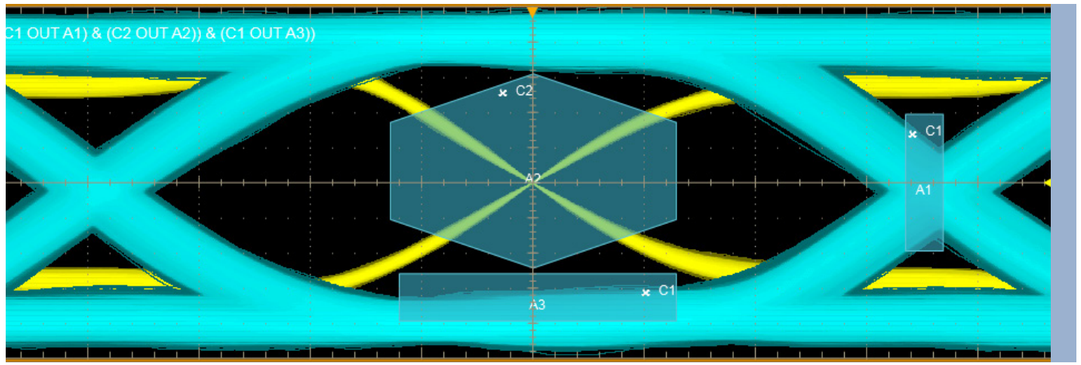
Tektronix®

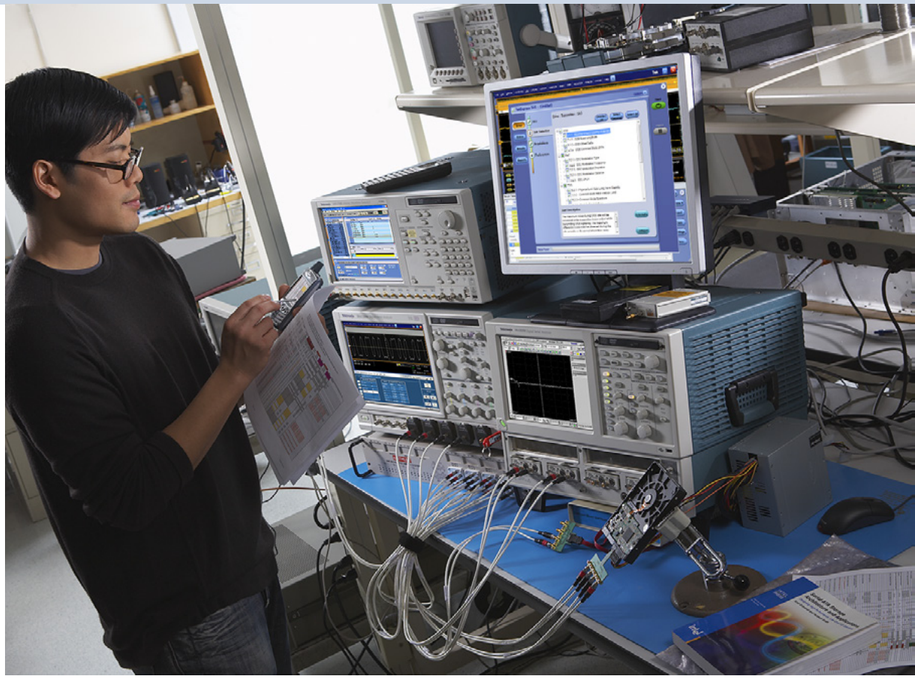
e-Guide to High Speed Interface Standards



PCI Express | DDR4 | USB | SAS/SATA

Introduction | High Speed Interface Standards

Next generation interface standards are pushing the limits of today's compliance and debug tools. Electrical validation of PCIe 4.0 16 Gb/s, SAS 12 Gb/s, SuperSpeed USB 10Gb/s, and DDR4 3200 MT/s and other high-speed bus technologies require even more complex test considerations than before. Transmitter performance, for example, is best evaluated with new analysis techniques that can accurately identify jitter & noise from sources such as crosstalk or other multi-lane noise coupling. With a closed eye architecture, commonly found in long channel designs, physical layer testing requires advanced techniques such as channel de-embedding and end-to-end link simulation with reference receivers.



Tektronix automation software simplifies the complexities of validating next-generation high-speed interfaces.

Design Challenges

- Smaller device geometries coupled with multi-layer PCBs incorporating buried via limit signal access
- Bus behavior with new power-saving schemes including frequency switching and clock gating
- Initiating test mode in-band through the channel, i.e., talk to the receiver's link training and status state machine
- Validating new signal encoding and equalization capability found in high-speed signaling interfaces
- Increasing complexity and quantity for electrical validation – so many tests, so little time!

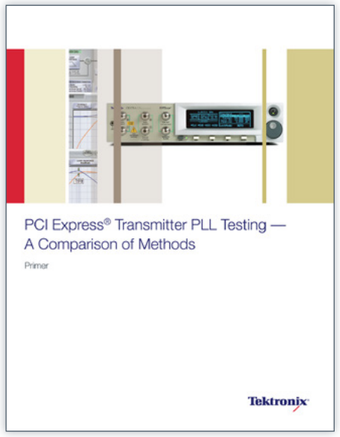
Standards

a. PCI Express
b. DDR4
c. USB
d. SAS/SATA

PCI Express | High Speed Interface Standards

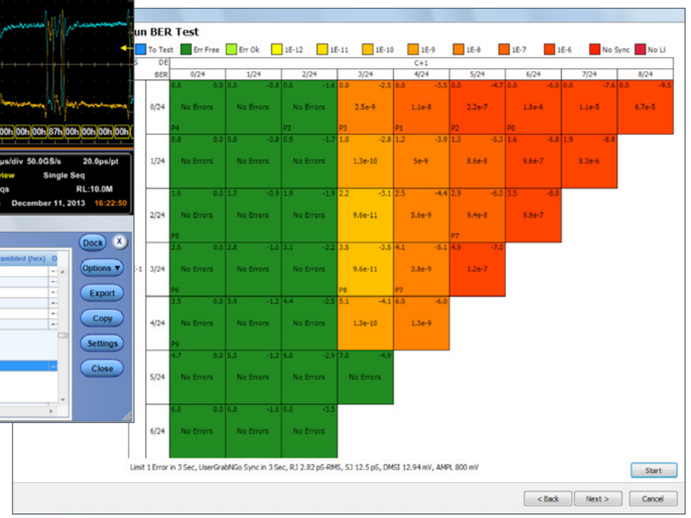
PCI Express is a high-speed serial computer expansion bus standard designed to replace the older PCI, PCI-X, and AGP bus standards. PCIe has a variety of improvements over the older standards, including higher maximum system bus throughput, lower pin count and smaller physical footprint. PCI Express recently released its 3rd generation specification to operate @ 8 Gb/s and work is underway to define the next or 4th generation specification targeted to operate @ 16 Gb/s.

PCISIG.com



Get our Primer on PCI Express® Transmitter PLL Testing – A Comparison of Methods

Observe PCI express link layer interactions using the oscilloscope's bus decode capability.



Observe receiver bit error map for all of the PCI Express' preset levels to assess BER margin.

Design Challenges

- Validating all bus speeds and presets per lane, for example, 8 Gb/s requires testing at 5 Gb/s and 2.5Gb/s with 11 de-emphasis presets on up to 16 lanes
- Placing the device into loopback to perform stressed receiver eye measurements
- Tracking link training sequences to validate speed and link width negotiation between transmitter and receiver

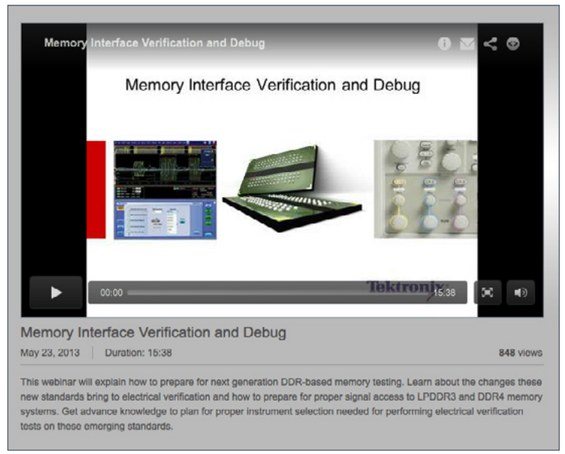
Tektronix Solution

- TekExpress for PCI Express automation software for in-depth compliance testing
- DPOJET and SDLA advanced link analysis for host and device system modeling
- BERTScope PCIe automation simplifies calibration and receiver tolerance testing
- TLA Logic Protocol Analyzer to trace and validate link layer behavior

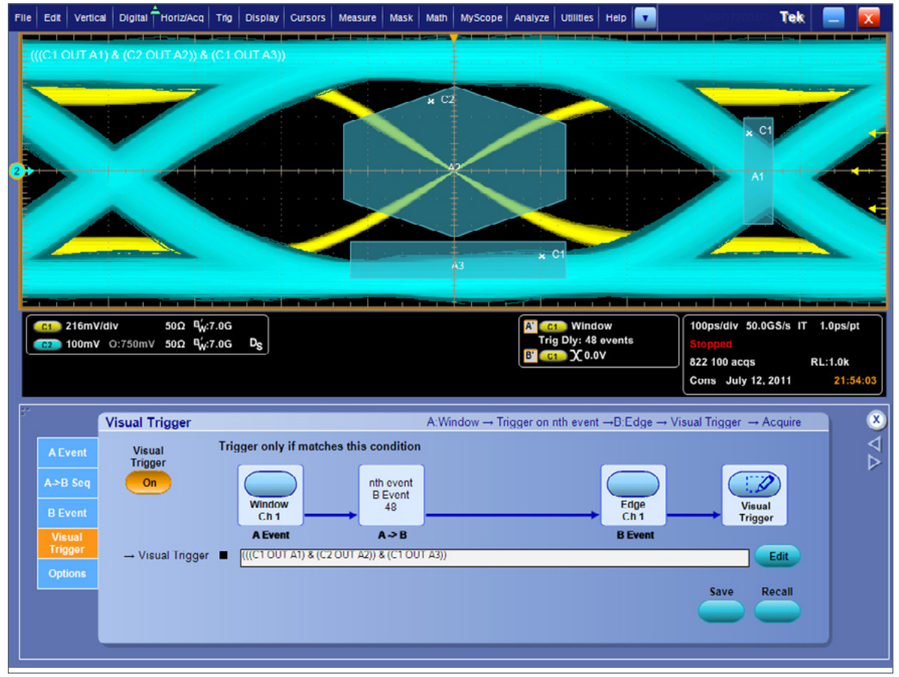
DDR4 | High Speed Interface Standards

DDR4 is the next generation memory standard targeted for enterprise computing. The standard enables higher capacity DIMM's (128 GB), doubles the data rate (3200 MT/s) and operates at lower voltage (1.2V) compared to the previous generation.

JEDEC.org



Watch our Webinar on Memory Interface Verification and Debug



Tektronix Visual Trigger can accurately capture fast reads & writes on DDR signaling

Design Challenges

- Signal Access for debug and validation
- Read / Write separation for analysis
- De-embedding to remove the effects of the interposer and probe, and to view signals @ the memory controller
- Triggering on error conditions such as data-dependent errors
- Protocol error checking

Tektronix Solution

- Interposer solutions enable signal access for both electrical and protocol validation
- DDRA automatically separates Reads / Writes then performs the relevant measurements
- SDLA enables generation of de-embed filters
- Visual Trigger can be used to define complex conditions, enables capturing conditions of interest
- The TLA7000 Logic Analyzer and the MCA5000 Memory compliance analyzers can be used to perform Logic validation and protocol compliance

CLICK HERE FOR DETAILED CONFIGURATION LIST AND TECHNICAL SUPPORT OPTIONS

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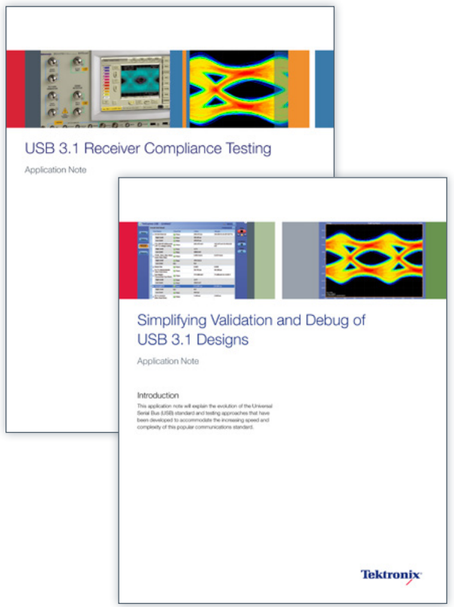
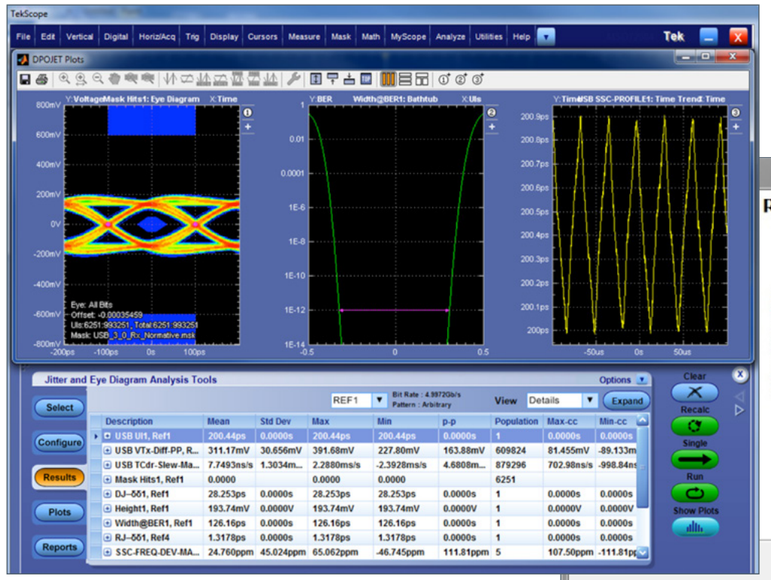


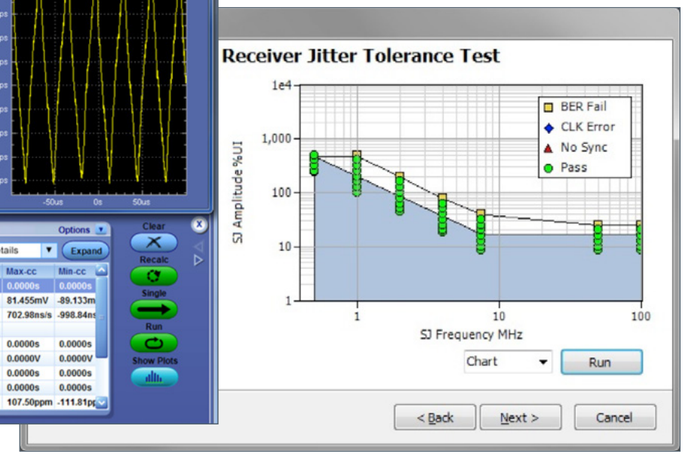
With the continued trend towards more bandwidth driven by larger and faster storage solutions, higher resolution video, and broader use of USB as an external expansion/ docking solution, USB 3.1 extends the performance range of USB up to 1GB/s by doubling the SuperSpeed USB clock rate to 10Gbps and enhancing data encoding efficiency. Additionally, the new USB Type-C connector greatly improves the user experience through high power, high bandwidth and more flexible usage.

USB.org

Get your FREE application kit for USB 3.1 Transmitter and Receiver Testing



Quickly perform USB3 transmitter eye, jitter, and timing measurements using Tektronix' automated USB3 analysis software.



Characterize your USB3 receiver performance with built-in jitter tolerance margin testing with the BSAUSB31 testing software.

Design Challenges

- Higher data rate means lower margins
- Long-channel signal recovery requires complex equalization
- 128b/132b encoding requires new LTSSM
- Backwards compatibility means more tests

Tektronix Solution

- DPOJET and SDLA advanced link analysis for host and device system modeling
- BERTScope USB 3.1 automation simplifies calibration and receiver tolerance testing
- TekExpress USB 3.1 Transmitter test software with comprehensive support for 5/10 Gb/s

Next-generation storage technologies such as 12 Gb/s SAS and SATA enable a new performance class of storage hierarchy that unlocks the performance of servers and solid-state drives.

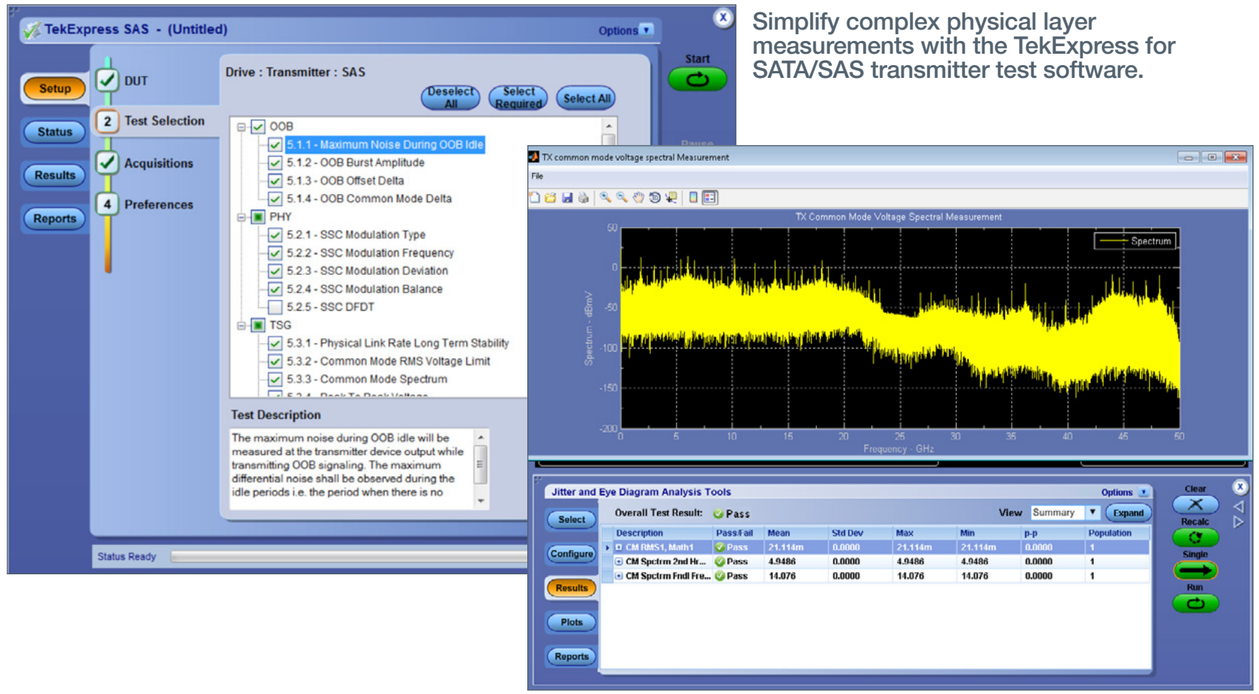
t10.org

scsita.org

sata-io.org

Methods of Implementation

- **SAS MOI**
- **SATA MOI**



Simplify complex physical layer measurements with the TekExpress for SATA/SAS transmitter test software.

Perform timing, jitter and amplitude analysis with DPOJET software

Design Challenges

- Complex bus topology and routing requires advanced equalization such as FFE/DFE.
- New host architectures include extensive Tx emphasis capabilities which can cause interoperability issues
- Independent clock domains require inclusion of logical idle characters between a transmitter and receiver

Tektronix Solution

- DPOJET and SDLA advanced link analysis for host and device system modeling
- BERTScope jitter tolerance search mode simplifies receiver margin testing while filtering align primitives
- TekExpress SATA/SAS Transmitter test software with comprehensive support for Tx equalization characterization

SATA SAS **CLICK HERE FOR DETAILED CONFIGURATION LIST AND TECHNICAL SUPPORT OPTIONS**

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Contact List Updated June 2013

For Further Information
Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit **www.tektronix.com**

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